Four Probe, *In Situ* Electrical Characterization of Dopant Structures in Silicon

Craig Polley

THE UNIVERSITY OF NEW SOUTH WALES

SCHOOL OF PHYSICS

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Abstract

In this thesis we demonstrate the *in situ* electrical characterization of planar, high concentration phosphorus layers in silicon close to the silicon-vacuum interface. To achieve this we have used an ultra-high vacuum four-probe scanning tunneling microscope (STM) in combination with a gaseous molecular dopant precursor (PH_3) and a silicon sublimation source for epitaxial encapsulation.

Initially we investigate and improve *ex situ* Ohmic contact formation to highly phosphorus doped silicon using nickel silicide rather than aluminium. We demonstrate improved reliability, depth control and the elimination of superconducting artifacts.

We develop a comprehensive understanding of how an *in situ* four-probe scanning tunneling microscope system can be applied for the measurement of electrical resistivity, both for bulk doped substrates and near-surface δ-doping profiles. Through extensive measurements we show that the sheet resistance of δ-doping layers can be reliably and unambiguously characterized, even at room temperature using conductive substrates.

Building on this, we then investigate the technologically relevant topic of how the resistivity of these degenerate 2D doping layers evolves as a function of their depth from the silicon-vacuum interface. We observe Ohmic conduction at depths as low as 0.5 nm, with a resistivity which sharply decreases from $\approx$24 k$\Omega/\square$ until saturating at $\approx$550 $\Omega/\square$ for depths beyond approximately 20 nm. Importantly, the sheet resistances we obtain at the depths we obtain them surpass all currently projected requirements from the International Technology Roadmap for Semiconductors (ITRS) for ultra-shallow junctions. We are able to explain the depth dependence with a conductivity model incorporating a finite segregation length of the grown layer combined with surface scattering.

Finally we extend this four-probe work towards the measurement of STM patterned dopant regions close to the interface. We obtain preliminary one-, two- and four-terminal resistance measurements on micrometer scale lithographically defined dopant patches. We highlight the challenges in such an endeavour, and show that probe-to-sample conductance measurements provide an unambiguous test of positioning accuracy.

Combined, using a four-probe STM we have built a solid experimental grounding for the understanding and further exploration of near-surface dopant structures in silicon.

Contents

Chapter 1

Introduction

In 1992 the cutting edge of personal computer processors was the Intel 486, which was built from an impressive 1.2 *million* transistors. Twenty years later, this introduction is being written with the help of an Intel Core i7 processor, which is built from 1.2 ***billion*** transistors. Advancement this rapid in any other field of engineering would be astonishing, but for computer processors it is simply 'business as usual'. The aggressive increases in transistor density have been consistent since the inception of integrated circuits in the 1960's, and as a result have become a defining characteristic of the modern semiconductor industry. The majority of people alive today have never known a time when computers did not become cheaper and faster every year.

And yet such a time will certainly come within our lifetimes, if not for engineering reasons then simply due to the discreteness of matter. Manufacturing is already at the '22 nm' node today in 2012; iterations through the '16 nm' and '11 nm' nodes are expected by 2018 but it is not clear that conventional planar transistor architectures are viable beyond this point[1]. At such length scales, transistor characteristics are strongly influenced by unavoidable effects such as quantum mechanical tunneling and the stray placement of individual atoms[2]. As a consequence, research efforts in computing technology today are divided between developing new tools and processes to extend planar CMOS scaling as far as possible ('More Moore') while also planning for radical new materials and information processing technologies ('More than Moore'). 'More Moore' involves advances in areas such as lithography, precision ultra-shallow doping and high-permittivity dielectric materials. 'More than Moore' is a broader topic; from a materials perspective it involves planning for the integration of new materials such as high-mobility or optically active III-V semiconductors, germanium and graphene. However it also encompasses entirely new approaches to information processing such as quantum[3,4], spin[5] or DNA[6] computing, often even going beyond Boolean logic. It is an exciting time to be involved in research.

An area critical to several of these research areas is the planar doping of semiconductors. The work in this thesis is based on the precision phosphorus in silicon doping scheme developed at UNSW by the Simmons group[7]. By exposing phosphine gas to a

clean, reactive silicon 2×1 surface in ultra-high vacuum (UHV) and heating the surface to 350°C, a self-limiting quarter monolayer of phosphorus is incorporated into the surface layer of the silicon crystal lattice. Low temperature epitaxial encapsulation of the dopants completes their crystalline environment and allows precise control over the depth of the doping plane from the silicon-vacuum interface. This doping process can be extended to include lithography by hydrogen passivating the reacting starting surface and selectively desorbing hydrogen atoms with a scanning tunneling microscope. The phosphine precursor then only adsorbs to depassivated areas of the surface, which can be created with atomic precision. Removing such samples from the UHV environment to add *ex situ* Ohmic contacts[8] enables low-temperature magnetotransport measurements of the nanoscale dopant 'devices'. To date this technology has been employed for the study of a variety of quantum electronic devices, including tunnel gaps[8], nanowires[9], Aharonov-Bohm rings[10] and perhaps most importantly quantum dots, which due to the strengths of the STM-lithography approach have been progressively and successfully scaled down to the limit of a single phosphorus donor[11;12;13]. The latter constitutes a key milestone in the realization of a scalable solid state quantum computer[14].

For the furtherance of planar transistor scaling, part of this thesis is dedicated to investigating the application of the Si:P δ-doping technique for ultra-shallow doping profiles in silicon. Such 'ultra-shallow junctions' are typically employed as part of the source and drain contacts in conventional planar transistor architectures, where they are crucial for the control of the 'short channel effects', negative operating characteristics which emerge as a consequence of aggressive downscaling. The Si:P δ-doping method, with its high doping densities ($\approx 2\times10^{14}\text{cm}^{-2}$), abrupt impurity profiles and atomic-resolution control of the encapsulation depth is ideal for investigating the limits of ultra-shallow junction scaling. We couple this with a novel *in situ* UHV four-point-probe STM system in order to electrically characterize these shallow doping layers while maintaining full control over the surface condition, allowing us to truly explore the physical limit of shallow doping technology.

Towards the development of novel 'post-CMOS' computing technology we develop an improved processing sequence for the creation of nickel silicide Ohmic contacts to Si:P dopant devices, solving problems related to reliability and low-temperature magnetotransport artifacts. We also lay the foundations for the four-probe *in situ* electrical characterization of STM-patterned dopant structures, building towards the long-term capability of measuring surface related structures such as molecules[15], nanowire interconnects[9] and even dangling bond logic gates[16].

Thesis outline

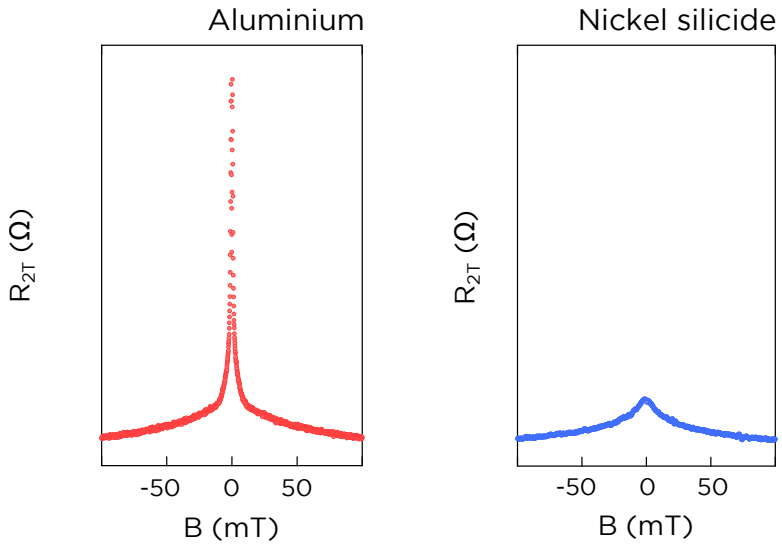
In **chapter 2** we develop an optimized Ohmic contacting scheme for STM-patterned buried dopant devices in silicon. Existing contacting methods for these devices use aluminium, which suffers reliability issues as well as superconductivity artifacts at the low temperatures used for quantum transport measurements. We show that many desirable properties of nickel silicide make it a leading candidate for a replacement, and proceed to develop a low temperature processing sequence for creating nickel silicide contacts to STM patterned devices. We perform extensive low-temperature comparative magneto-transport measurements to verify the improvement over aluminium contacts.

Chapter 3 is concerned with the application of a novel characterization technique - the *in situ* nanoscale four-point probe - to measuring the room temperature resistivity of near surface Si:P δ-doping profiles in silicon. We develop a comprehensive understanding of the nanoscale four-probe tool and how it can be applied to unambiguously determine the resistivity of both bulk and δ-doped silicon samples. In particular, we show conclusively that despite the use of conductive substrates, electrical measurements with this tool can be used to measure the resistance of the δ-layer only, due to spreading resistance effects.

In **chapter 4** we apply our newly developed knowledge to study the *in situ* resistivity of Si:P δ-layers as a function of the vertical distance of the doping profile from the silicon interface. Such layers can be considered 'ultimate' versions of the ultra-shallow junctions critical to future transistor scaling. Measuring the resistivity for depths ranging from 20 nm all the way down to 0 nm with ångstrom resolution, we report values of sheet resistance which surpass all currently projected ITRS requirements (out to 2015). We provide a physical model for the observed depth dependent conductivity based on segregation and surface scattering, which closely matches experimental data.

Chapter 5 aims to further extend the combination of *in situ* four-probe and near-surface Si:P δ-doping by electrically characterizing lithographically defined dopant regions. We provide important verification that current passed through a dopant pattern at room temperature remains confined to that pattern and does not spread through the underlying substrate. We also demonstrate that probe-to-sample current-voltage measurements display a unique and unambiguous conductance feature when placed over a dopant patch, and that this can be used to verify the accuracy of probe positioning. Building on these findings, we show preliminary measurements of micrometer-scale dopant patterns.

Chapter 6 summarizes the outcomes of the thesis and offers a roadmap for future research to build on the work presented here.



A nickel silicide contacting scheme for δ-doped silicon

Index of key results and discussions

For introductory material covering what an STM-patterned device is and how the existing contacting scheme can be problematic, refer to section 2.1 on page 7.

For discussion of what limitations STM-patterned devices impose, what the possible Ohmic contacting schemes are and why nickel silicide has been chosen for further study, refer to section 2.2 on page 13.

Section 2.3 deals with the development of a nickel silicide processing recipe compatible with STM patterned devices. For a review of the literature regarding nickel silicide formation, see section section 2.3.1 on page 23. For the final developed recipe, see page 31.

Section 2.4 contains comparative electrical measurements of samples contacted by nickel silicide and by aluminium. The contact resistance (page 36) and phase coherence properties (page 38) are comparable, while the superconductivity artifacts are eliminated by using nickel silicide (page 40). We also demonstrate that while rate dependent magnetic field hysteresis is present in both samples, it is not related to the use of nickel silicide (page 45).

For a journal article summarising the results of this chapter, see reference[17] - Polley *et al*, Nanoscale Research Letters **11** 2272 (2011).

2.1 Introduction

This chapter is concerned with developing an optimal Ohmic contacting scheme for STM-patterned dopant devices. In this section we provide the necessary context of what an STM-patterned device is and what limitations they impose on the formation of Ohmic contacts. We then highlight shortcomings of the existing aluminium based contacting scheme, motivating the work of this chapter.

Hydrogen-resist scanning tunneling microscope (STM) lithography as a means to pattern Si(100) 2×1 surfaces with adsorbates was pioneered by Lyding in 1994[18]. This technique has been adapted by the Simmons groups at UNSW over the past decade, and today is capable of atomically precise, arbitrarily complex dopant placement in silicon[13]. Within the Simmons group the main application of this technology has been electrical and spin transport studies of nano- to atomic-scale phosphorus dopant patterns in silicon. This necessitates macroscopic electrical connections to the dopants, which is challenging for several reasons:

- The dopants are buried under ≈25 nm of high resistivity silicon before removal from the ultra-high vacuum (UHV) environment, necessary to activate the dopants and avoid complex surface interactions.
- Alignment tolerances are tight due to the small size of the dopant structures - the largest features created by STM lithography are a few square micrometers.
- STM patterned regions are not usually visible to optical, electron or scanning probe microscopy once buried and removed from vacuum.

The ability to make electrical contact to buried STM-patterned dopant structures was developed in 2004 by both Rueß[19] and Shen[20] independently. The method of Rueß has been employed extensively since this time and is the subject of continual refinement as the complexity of dopant devices continues to grow. The focus of this chapter will be contributing to this ongoing optimization by examining an alternative metallization strategy. Specifically, we seek to find a viable replacement for the existing standard, aluminium, which is known to exhibit superconducting properties at low temperatures.

2.1.1 An overview of STM device fabrication

Before discussing the problems with aluminium which motivate this work, we will first briefly review the process of creating and contacting an STM patterned dopant device as

outlined by Rueß[19] and Füchsle[21]. With reference to Figure 2.1,

(a) Devices are fabricated on commercially available silicon (100) substrates with low miscut angles ($\pm 0.1^{\circ}$) and light background doping (1-10 Ωcm). Some level of doping is important for subsequent heating and STM imaging stages, but it must be sufficiently low that the substrate does not conduct at liquid helium temperatures.

(b) *Registration marker* patterns are etched into the substrate. By aligning subsequent patterning steps to these markers, the patterned regions can be relocated with the STM when necessary[19;21].

(c) The substrate is loaded into ultra-high vacuum, where it is direct current heated for short periods (*flash annealed*) to obtain a clean 2×1 surface reconstruction (after the method of Swartzentruber[22]). This surface is then terminated with atomic hydrogen to act as a resist layer for subsequent STM patterning[18].

(d) An STM tip is used to selectively desorb hydrogen and create reactive dangling bond sites, with the potential to achieve single atom resolution[23]

(e) The surface is dosed with phosphine gas, with PH_3 molecules selectively adsorbing to exposed dangling bond sites. Due to the high density of surface states and the small footprint of the phosphine molecule, extremely high doping densities can be achieved ($\approx 2.0\times10^{14}\text{cm}^{-2}$)[24]

(f) A short duration low temperature anneal dissociates the phosphine and incorporates phosphorus atoms into the top layer of the silicon lattice[25].

(g) The surface is buried under $\approx$25 nm of epitaxial silicon, serving to both complete the crystalline environment for the dopants and protect them from surface effects prior to removal from UHV. We will have much more to say about surface effects in chapter 4

(h) With *ex situ* processing, Ohmic contact is made to the buried dopant structure by patterning aluminium leads onto the surface. After furnace annealing the aluminium spikes down through the substrate and makes contact to the underlying dopant device, as we will discuss shortly. The aluminium leads are then wire bonded to a carrier package for electrical characterization.

The original decision by Reuß to use aluminium was motivated by its possession of several desirable properties. In approximate order of importance:

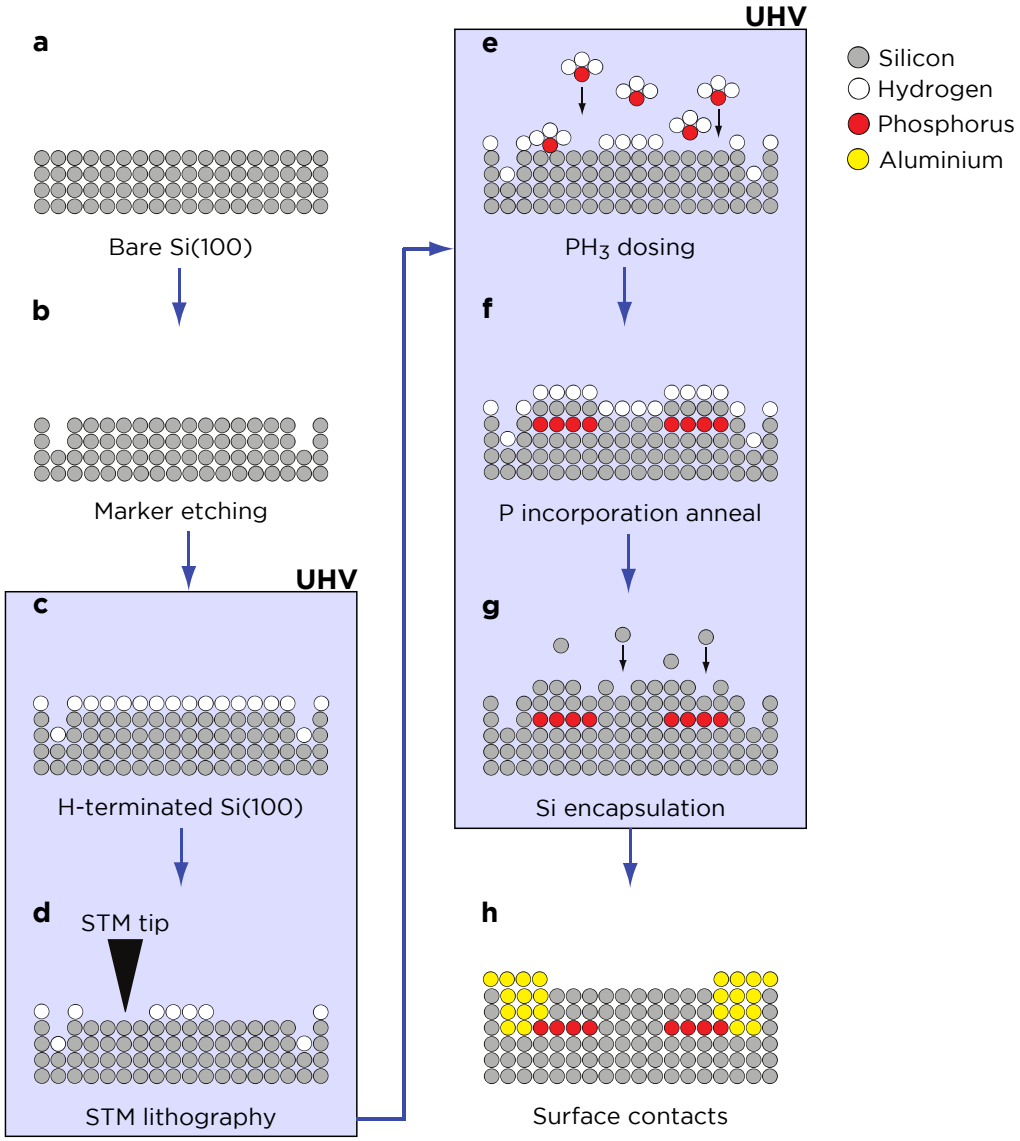


Figure 2.1: **Atomic-scale device fabrication with STM** A schematic of the fabrication process for an STM-patterned dopant device, as described in the main text (*Adapted from Pok*[26])

- It is easy to process. Aluminium can be deposited by a single-step thermal evaporation, has good adhesion to silicon and will form reliable wire bonds.

- It is very well studied and documented, having been used as an Ohmic contact to silicon since the inception of silicon integrated circuits in the 1960s

- It is a good electrical conductor. With a bulk resistivity of 28 nΩm, at a thickness of 80 nm one expects a sheet resistivity of 0.35 Ω/□. As a connection to devices that are typically kΩ to MΩ this is perfectly acceptable.

2.1.2 Limitations in the existing contacting process

Despite a history of successful application to atomic-scale devices, there are several indications that aluminium is not an optimal metallization. In the following sections we will discuss specific circumstances under which aluminium can prove troublesome.

2.1.2.1 Magnetotransport artifact from superconducting contacts

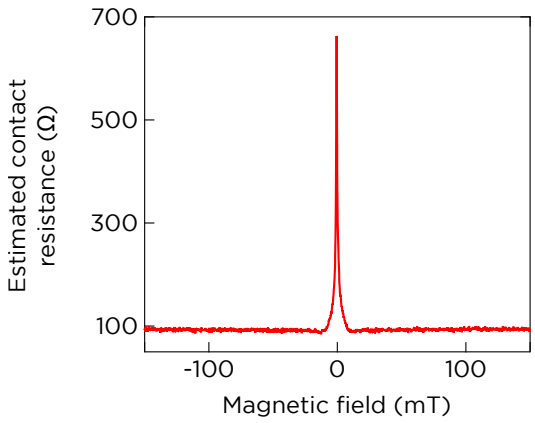


Figure 2.2: **Superconductivity artifact** An example of the spike in contact resistance observed when using superconducting aluminium contacts. This data is recorded at 100 mK from a δ-doped Si:P Hall bar structure using aluminium contacts.

At the milliKelvin temperatures where most quantum electronic devices are measured, aluminium becomes a superconductor. For the typical thicknesses employed as a thin film contact (≈60 nm), aluminium retains bulk superconducting properties - namely a critical temperature T_C of 1.17 K and critical magnetic field B_C of 11 mT. The consequence of this behaviour is a spike in the two-terminal resistance as illustrated in Figure 2.2. We will discuss the mechanism behind this effect in later sections; for now we simply note that such a feature restricts zero-field measurements and complicates the analysis of two-terminal magnetotransport data.

2.1.2.2 Unreliable depth control

In the final step of Reuß's contacting scheme aluminium is evaporated onto the sample surface, but this alone will not create an Ohmic contact. The dopant structure resides some tens of nanometers below a high resistivity silicon encapsulation layer; at such a separation there is negligible coupling to the aluminium. To bring the aluminium closer to the dopants a low temperature furnace anneal (350°C for 30 minutes) is performed. At this temperature silicon has a non-negligible solubility in aluminium ($\approx 0.13\%$, see Figure 2.3a). In localised areas silicon will dissolve into the aluminium, leaving behind pits which are then filled with aluminium. This is the 'spiking' phenomenon, a bane of early microelectronic manufacturing. But for buried dopant devices such an effect is precisely what is required - the annealed aluminium spikes through the encapsulation layer and makes good contact to the buried dopants. The problem lies with the highly random nature of the spiking events, both in distribution and depth. A successful contact requires a sufficiently deep spike within the few square microns of overlap with the buried dopants. The low yield and effectively random contact resistance which results causes significant problems for device fabrication.

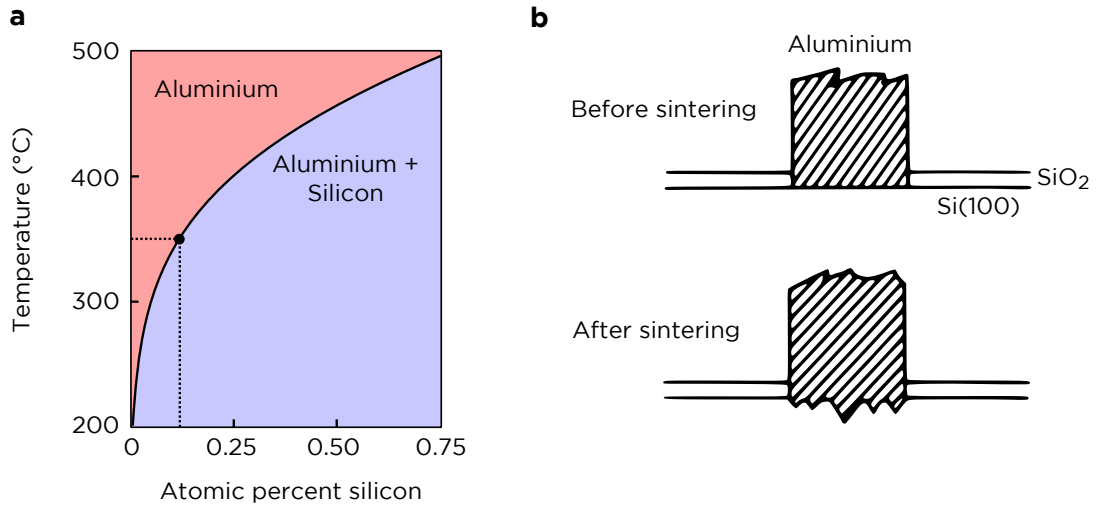


Figure 2.3: **The spiking effect for annealed aluminum-silicon contacts** (a) The aluminium-silicon phase diagram, showing a non-negligible solubility of Si into Al at 350°C (*Adapted from Murray & McAlister*[27]). (b) Schematic cross-section of an aluminium-silicon contact before and after annealing. Random pitting of the silicon occurs (*Reproduced from Runyan & Bean*[28]).

2.1.2.3 Rate dependent magnetic-field hysteresis

Rate dependent hysteresis* in magnetoresistance measurements is commonly observed in milliKelvin transport measurements; we show two examples in Figure 2.4. In Figure

Rate dependent denotes that the hysteresis stems from a transient response rather than bistability.

2.4a the measured magnetoresistance of a δ-doped Hall bar sample differs depending on the direction of the magnetic field sweep, as indicated by the red and blue traces. Figure 2.4b shows a similar effect observed for a silicide nanowire[29]. Such an effect typically originates from magnetic material in the vicinity of the device, either through residual magnetization, eddy current heating or adiabatic demagnetization[29]. As a superconductor, aluminium is a perfect diamagnet and does not cause such effects, but this artifact does highlight the need to select nonmagnetic materials when choosing an alternative. Avoiding rate dependent hysteresis requires long measurement times, and complicates curve-fitting. We will discuss hysteresis effects in greater detail in a subsequent section.

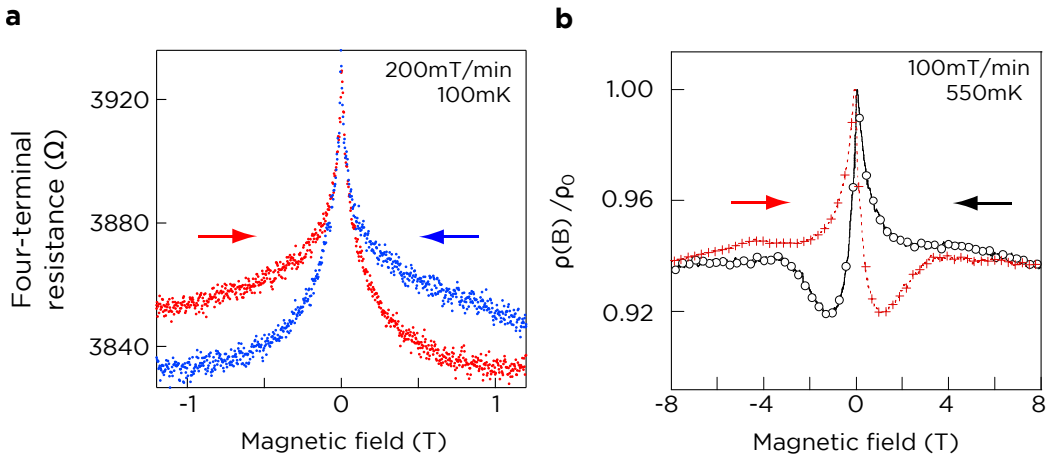


Figure 2.4: **Hysteretic effects in a changing magnetic field** Examples of milliKelvin hysteresis artifacts seen when measuring magnetoresistance at high sweep rates of the magnetic field. In (a) we show the magnetoresistance of a δ-doped Si:P Hall bar structure from later in this chapter. In (b) we reproduce a measurement of Kim *et al* on a silicide nanowire[29], where the hysteresis stems from paramagnetic moments in the surface oxide of the wire.

2.1.2.4 Reliability

At the final stage of processing, wire bonding is required to make the connections from the microscopic silicon device sample to the macroscopic contacts of the chip package. Typically aluminium wedge bonding is used, and in terms of adhesion and contact resistance the bonding process is very reliable. Samples are measured at cryogenic temperatures once processing is complete, but occasionally must be remeasured months or years later. There have been cases where this is found to be impossible due to severe degradation of the contacts. Since these are pure aluminium-aluminium bonds with no intermetallics or adhesion issues, the most likely explanation for this degradation is the severing of cracks in the wedge heel[30] due to fatigue from the extreme thermal cycling ($\approx$ 300 °C). Irrespective of this behaviour, it is necessary to move away from aluminium bonding to address the superconductivity artifacts discussed above. However such re-

liability problems underscore the need to be mindful of both metallization-to-bond and metallization-to-sample behaviour, as both can be problematic when bonding[30].

2.2 Choosing an optimal Ohmic contact metallization

Having established the motivation to move away from aluminium as an Ohmic contact metallization, in this section we discuss the considerations in selecting an alternative. We first review the relevant aspects of metal-semiconductor contact physics, and follow this with a discussion of the advantages and limitations imposed by the STM-patterned dopant device architecture. Having provided this context, we then review potential candidates and rationalize the choice of nickel silicide

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2.2.1 Overview of a generic metal-semiconductor contact

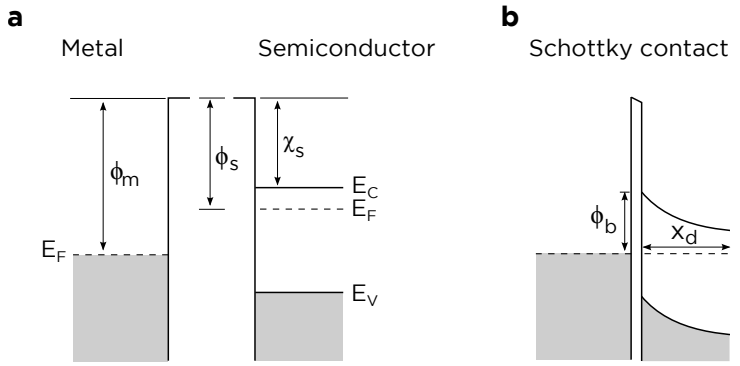

Figure 2.5: **The formation of a metal-semiconductor Schottky barrier** (a) A schematic band diagram of a metal and an n-type semiconductor, both electrically neutral and isolated from each other. (b) The equilibrium state when these two materials are brought into close contact. Band bending in the semiconductor results in the characteristic Schottky barrier ϕ_b, which extends over a distance x_d into the semiconductor.

When a metal is brought into contact with a semiconductor, a rectifying electrical contact is the usual outcome (i.e. the degree of electrical conduction through the junction depends on the polarity of the applied bias). This observation was first recorded in 1874, and even without an understanding of the mechanism it readily found practical application in early work on radio communication. Metal-semiconductor contacts have remained relevant in technology over the last ≈140 years, and as a consequence our understanding of their behaviour has advanced tremendously. For this chapter it will be sufficient to introduce the simple physical model of Schottky and Mott from 1939. However the behaviour of metal-semiconductor junctions is crucial to interpreting many of

the observations in this thesis, and we will return to the topic several times when a more advanced treatment is required.

The starting point for understanding metal-semiconductor junctions is the formation of the *Schottky barrier* responsible for inhibiting carrier transport. In Figure 2.5a we show schematic band diagrams for an arbitrary metal and n-type semiconductor, applicable to the samples in this chapter. With reference to Figure 2.5a, the work function ϕ of a solid is the minimum amount of energy required to remove an electron from the Fermi level to a point outside the surface of the solid. A related parameter is the electron affinity of a semiconductor, χ_s, which follows the definition of work function but is referenced to the bottom of the conduction band. To illustrate the origin of a Schottky barrier, consider what must occur when we bring the two materials in Fig. 2.5a together as in Fig. 2.5b.

1. As a prerequisite of establishing equilibrium, the two materials will exchange carriers until their Fermi levels align. Recall that the Fermi level indicates the highest occupied energy state of electrons; if it were not flat across the junction the implication would be that electrons on the higher side *could* lower their energy by diffusing to the other side, but for some reason *have not* - this would not then correspond to equilibrium.

2. As electrons traverse the junction, their positively charged donor atoms remain behind, locked into the crystal lattice. The charge separation establishes a retarding electric field, causing electrons to drift back to their host. At the drift-diffusion equilibrium, some charge-imbalance still remains

3. How is this unbalanced charge spatially distributed? The density of free electrons in a metal is enormous, and can readily redistribute to compensate extra charge within a *screening distance* of less than a nanometer. In a semiconductor the free carrier densities are many orders of magnitude lower, so the *space-charge* region of uncompensated donor extends over an appreciable distance, typically 10 - 100 nm. This is illustrated in Fig. 2.5b

4. The potential step ϕ_b and gradual field decay into the semiconductor are called the Schottky barrier.

In the simplest model, the height of this barrier is given by:

$$\phi_b = \phi_m - \chi_s$$

while the width of the barrier x_d can be shown by electrostatic analysis to be proportional to both its height and the semiconductor doping:

$$x_d \propto \sqrt{\frac{\phi_b}{N_d}}$$

Electrical transport across the Schottky barrier can occur via thermal excitation of carriers over the barrier (*thermionic emission*), quantum mechanical tunneling through the barrier (*tunneling*) or a combination of the two (*thermionic field emission*). When we apply a voltage to a metal-semiconductor junction, it is the height of the Schottky barrier which we directly alter. Thus when the dominant conduction mechanism involves going over the barrier, voltage dependent conductance (rectification) results. When tunneling is the dominant mechanism it is only the barrier *width* which is relevant[†], so we obtain voltage-independent (Ohmic) conductance.

This is a simplified treatment of the physics of metal-semiconductor junctions, but is sufficient to provide the background for this chapter. Based on the discussion so far, we can already make a key observation regarding a contact scheme for δ-doped Si:P structures. The width of the barrier scales as $1/\sqrt{N_d}$, so for the extremely high doping density of $\approx 10^{21}$ cm^{-3} the barrier will be so thin as to place any metal-semiconductor contact firmly in the tunneling regime, regardless of the Schottky barrier height. In contrast to the majority of Ohmic contact development work, this allows us to remove the emphasis on barrier height and instead focus on more unconventional requirements. We will now discuss these requirements.

2.2.2 Requirements and limitations

Our goal is to develop an electrical contacting process which results in Ohmic, low resistance contacts to our Si:P n-type δ-doped devices. What constitutes 'low resistance' depends on the context. In conventional microelectronics specific contact resistivities of less than 100nΩcm^{-2} are required to realize aggressively scaled speed and power consumption targets[1]. In the present context of characterizing δ-doped devices we have simpler criteria; essentially we only require that the contacts do not contribute appreciably to any measured or extracted parameters. While lower contact resistance is always better, device resistances are typically upwards of 10kΩ; as such a total Ohmic contact resistance of $\approx$1kΩ would still be considered acceptable.

The chief considerations when designing a contacting scheme are therefore:

- The lowest thermal budget possible, to limit the diffusion of precisely placed dopants. To give an estimate for these requirements, a previous study has calculated that to maintain a dopant diffusion length of less than two silicon lattice sites during a 3 hour anneal, a temperature of less than 300°C must be maintained[31].
- An absence of ferromagnetic material (to avoid introducing hysteresis)
- An absence of superconducting material (to avoid superconductivity artifacts)
- Practical to implement - this encompasses availability, toxicity/radioactivity, processing equipment required and stability in both air and water

[†]Strictly speaking the barrier width is also changed when the barrier height changes, but only weakly

- The ability to physically reach the buried dopant layer, either through solid-state reaction or with the assistance of vias. This is required to minimise the barrier width that carriers must tunnel through.

As discussed earlier, the extremely high doping levels within the δ-layer relax the usual requirement of selecting a material with low barrier height to n-type silicon.

2.2.3 Candidate schemes

To design a contacting scheme we first take an abstract view of the process, which can be divided into two parts. The first task is to create an Ohmic electrical contact to the nanoscale buried dopant layer with a larger area conductor ($> 100\ \mu m^2$). The second task is making a wire bond from this intermediary conductor to a macroscopic carrier package ($\approx mm^2$).

The first and most challenging aspect - contacting the dopant structure - presents two major difficulties. After identifying and aligning subsequent processing to the nm-scale buried structure[19;21], we must be able to make good electrical contact through the 25+ nm silicon encapsulation layer to a contact region with an area of only a few square microns. The second aspect - making a wire bond to this first level of contact - is more straightforward, simply requiring appropriate metallurgy to create a reliable and stable bonding connection. The standard approach is the deposition of a metal bond pad; bonding directly to silicon is sometimes possible but not mechanically reliable[30].

2.2.3.1 Selecting a suitable metal

We discuss first the considerations in choosing a bonding metallurgy, since this requirement is common to all contacting schemes. In Figure 2.6 we show the superconducting transition temperatures of known elemental superconductors. To avoid the magnetoresistance artifacts discussed earlier, it is important to select materials which are not superconducting at the temperatures used for characterization (also indicated in Figure 2.6). Guided by this figure we can already eliminate a large portion of the periodic table as shown in Figure 2.7. We can also eliminate the ferromagnetic elements iron, cobalt and nickel in order to avoid introducing hysteresis. Finally, certain elements can be eliminated on the basis of practicality - for example mercury is liquid at room temperature, scandium reacts violently with water and thallium is highly toxic.

Since an aluminium bond wire will also superconduct, gold wire bonding should be used. On the basis of interface reliability with gold wire bonding, gold or silver are the most appealing of the remaining candidates in Figure 2.7[30]. Of these two, gold is the first choice due to its superior corrosion resistance. However both gold and silver have poor adhesion to silicon[33]. The usual solution to such problems is the use of a two-layer metal stack, where the first is a thin (few nm) layer chosen for adhesion to silicon. Common metals for this purpose are titanium or chromium[34]. We note that the superconductivity

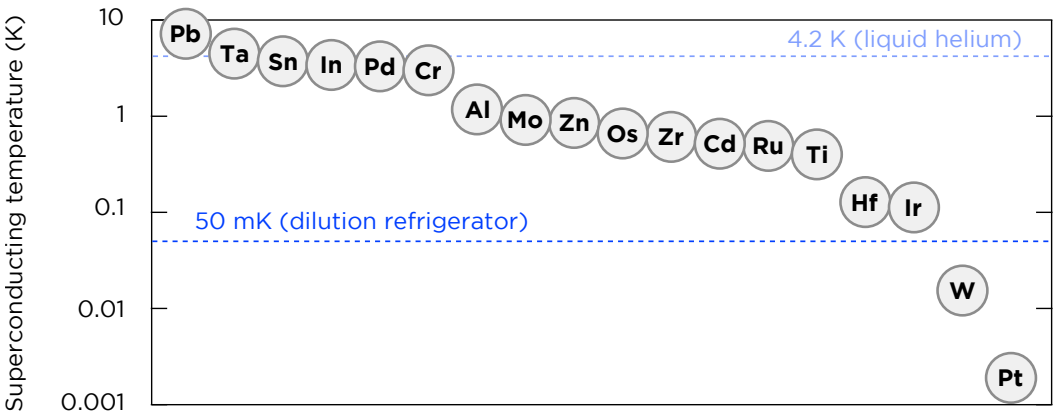

Figure 2.6: **Transition temperatures of the elemental superconductors** Values of the superconducting transition temperature for common elemental metal superconductors at atmospheric pressure. For context, temperatures corresponding to a liquid-helium dip station and a dilution refrigerator are marked. (*Critical temperatures from Burns*[32])

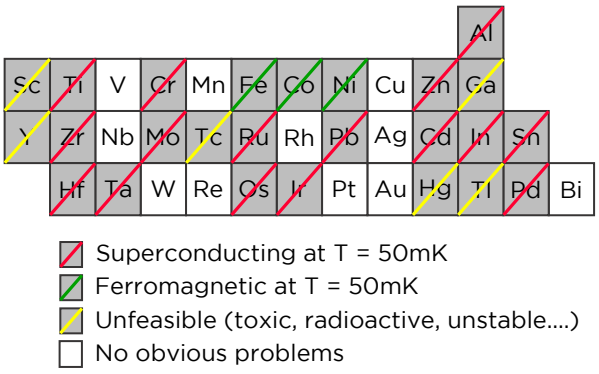

Figure 2.7: **Selecting an appropriate metal** The relevant section of the periodic table for choosing a suitable metal for creating bond pads. Eliminating elements with obvious problems for cryogenic magnetotransport measurements (shaded) leaves only a few candidates.

of these elements does not necessarily preclude them from this application, as very thin layers of material (below ≈10 nm) often exhibit reduced or eliminated superconductivity due to the proximity effect. While the adhesion layer can be very thin, the overall bond pad should be as thick as possible to minimise damage to the substrate while bonding[30].

We now move on to discussing the first consideration in our abstracted contacting scheme, which is the problem of making good contact to a *buried* dopant plane.

2.2.3.2 Vias

The most obvious approach to this problem would be to simply etch a hole through the encapsulation layer and backfill it with a metal, mirroring the via process in microelectronic manufacturing. Indeed, in parallel with this candidature other workers have developed and adopted such a method within the Simmons group (Figure 2.8). Electron beam lithography and reactive ion etching is used to define an array of ≈ 70 nm deep holes over the buried contact regions, with typical hole diameters of 150 nm and a pitch of 500 nm. This hole diameter is essentially the smallest that can be accomplished without introducing complicated process steps; the sub-30nm tungsten studs in Figure 2.8b require sidewall plating and surface passivation during etching. The ratio of hole diameter to pitch is a compromise between maximising the contact area and leaving enough of the dopant layer to maintain acceptable sheet conductance. An *array* of holes is used to maximise the odds of successfully contacting the buried layer.

In addition to having a high success rate, the via technique has the advantage of the lowest possible thermal budget as no post-metallization anneal is required. The limitations of the technique are set by the quality of etching available. With the present minimum hole diameters (≈150 nm) and alignment accuracy the smallest contactable area is approximately 500 nm × 500 nm, while the depth control for the etch limits the ability to selectively contact stacked dopant layers.

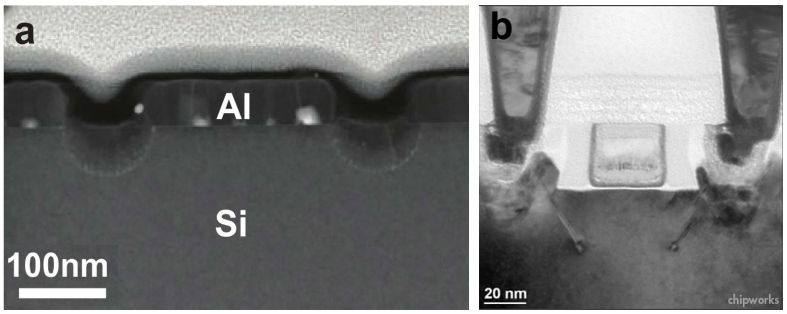

Figure 2.8: **Vias for contacting buried structures** Cross sectional electron microscope images of (a) the aluminium via contacting scheme currently in use within the Simmons group[35] and (b) a transistor from Intel's 32nm process line showing the first level of vertical interconnects[36])

2.2.3.3 Pre-defined doped contacts

A very different approach to the problem is the creation of highly doped regions in the substrate *before* entry into UHV. This can be accomplished either through furnace diffusion[37] or ion implantation[20]. At the STM patterning stage one would then align the lithography to the highly doped regions. A subsequent metallization stage is still required to contact the pre-doped regions (which are now buried with the device); a description of this step was omitted from references[37] and[20], but could easily be accomplished with the previously discussed via technique.

Defining doped contacts prior to STM lithography has two main advantages which follow from the relative ease of making arbitrarily large doping regions. One is that it overcomes the problem of long times being required to create large area (on the order of square microns) contact patches with a desorption tool (the STM tip) designed for atomic-resolution lithography. By preparing large area contacts in advance, the device fabrication process could in principle be greatly optimized. Secondly, it would also make the second contacting stage (e.g. via creation) much easier by virtue of having a larger area to contact.

However the additional processing steps involved in fabricating highly doped contacts increase the difficulty of obtaining the clean, defect-free starting surfaces critical for atomic-scale device fabrication. As demonstrated in[20] this is not an insurmountable problem, but it complicates the task of obtaining a high-quality surface. A second disadvantage is one of flexibility; pre-defined contacts limit the freedom to alter the placement of leads if surface conditions change during patterning. This limitation becomes especially important as device structures become complex and the number of terminals required increases.

2.2.3.4 Hydrogen desorption by electron microscope

Access to a reliable, high-throughput means of hydrogen lithography would offer another alternative, with all the advantages of pre-defined contacts. Large area contacts to small STM patterns could easily be created by lithographically patterning them *in situ* on the same atomic plane and dosing with phosphine. Proof of principle that an *in situ* scanning electron microscope can satisfy this purpose has been demonstrated by Hallam *et al* in the Simmons group[38]. Using a beam energy of 25 keV, hydrogen desorption of a 4×4 μm square with $\approx$ 200 nm resolution was demonstrated. The quality of desorption was such that a free carrier density of $8.2\times10^{13}\text{cm}^{-2}$ was obtained after δ-doping. While only $\approx$30% of the maximum demonstrated density of $2.4\times10^{14}\text{cm}^{-2}$[39], this is still sufficient for metallic conduction. The electron microscope technique is promising, but would require further optimization to improve resolution and reduce stray desorption and contamination from the electron beam.

2.2.3.5 Silicides

The final approach we will discuss for contacting buried layers is the use of a silicide contact. The term *silicide* most commonly refers to a compound of silicon and metal, which is typically created by a solid state reaction between a silicon substrate and metal overlayer. Growth of the silicide proceeds downwards into the substrate in a controlled manner, making it an interesting candidate for contacting buried dopant structures.

Silicides are nearly always good electrical conductors, and have attracted considerable research attention over the last ≈ 50 years as an Ohmic contact or interconnect material for CMOS (Complementary Metal Oxide Semiconductor) manufacturing. The silicide reaction can be masked by silicon dioxide, a fact capitalised on in microelectronic manufacturing to automatically align contacts with source-drain regions implanted through an oxide window. The metal precursor can be blanket deposited, with silicide forming only within the windows in the silicon dioxide; excess unreacted metal can be selectively stripped with subsequent chemical treatment. In this application the silicide is often referred to as a salicide (**s**elf **a**ligned si**licide**). Since the 1960's this application has motivated and guided the now considerable body of research into silicide reactions.

Silicides can be divided into three groups based on the position of the metal reagent in the periodic table - refractory, near-noble and rare earth. General trends in the metallurgy can be observed for the three different groups. In order to evaluate leading candidates for contacting buried dopant devices, we will briefly discuss these trends and some notable examples. A summary of important material parameters is provided in Table 2.1.

Refractory silicides (groups IV - VI) typically form disilicides (ASi_2) as a first phase, with formation temperatures of around 600°C. During growth the silicon is the dominant diffusing species. **$TiSi_2$** is the most notable member of this group, being the replacement for aluminium as a CMOS contact metallization in the 1980s[40;41]. It has low resistivity and good thermal stability, but more importantly it successfully solved the spiking and electromigration issues of aluminium with the additional benefit that titanium is a strong reducing agent. This relaxes some of the processing constraints with respect to oxygen levels during growth and native oxide removal. $TiSi_2$ exists in two allotropic phases according to the annealing conditions of the silicidation, a high resistivity C49 phase ($60\mu\Omega$cm) and a subsequent, lower resistivity C54 phase ($15\mu\Omega$cm). This transition is nucleation limited, with the consequence that the transition becomes progressively more difficult to attain as the contact size is reduced. High temperature rapid thermal anneals can help, but eventually become impractical. This led the CMOS industry away from $TiSi_2$ in the 1990s.

Near-noble silicides (group VIII - X) form a metal-rich silicide (A_2Si) as a first phase at around 200°C. The subsequent, typically lower resistivity monosilicide (ASi) or disilicide (ASi_2) phases can be obtained with higher temperature anneals (see Table 2.1). During growth the metal is the dominant diffusing species. For microelectronics processing,

$CoSi_2$ was the replacement for $TiSi_2$, having comparable electrical properties (15$\mu\Omega$cm) but without seeming to possess the same difficulties at small feature sizes. In fact such difficulties did eventually arise for features sizes below 50nm. In addition as a disilicide it consumes a lot of silicon, making it inappropriate for newly emerging SOI substrates or ultra-shallow junctions. **NiSi** is the replacement for $CoSi_2$ beyond the 65nm manufacturing node[42]. It has a resistivity comparable to $TiSi_2$ and $CoSi_2$ (10 $\mu\Omega$cm), but forms at lower temperatures, consumes less silicon during formation (as a monosilicide) and integrates well with emerging Ge and SiGe substrates. The formation is diffusion-controlled, giving a highly uniform planar growth front. It suffers from a reduced thermal stability, either agglomerating or converting into the disilicide phase for temperatures exceeding $\approx$ 800°C. **IrSi** is noteworthy for having the lowest known barrier height to p-Si at 0.17 eV. Hence it attracts attention for complementary Schottky barrier MOSFET architectures, which require materials with low barrier heights to both p- and n-Si.

Rare earth silicides form disilicides as a first and typically only phase at around 350°C[43]. They reach this disilicide phase at lower temperatures than both refractory and near-noble silicides, and also feature the lowest known barrier height to n-Si. No member of the other two silicide classes can obtain a barrier height to n-Si lower than half the Si bandgap ($\approx$0.55 eV). All of the rare earth silicides possess magnetic ordering at cryogenic temperatures, a consequence of the incomplete 4f orbital states. Of this class of materials **$ErSi_2$** is the most well studied.

Table 2.1 provides a broad overview of the literature concerning important silicide characteristics, the most important of which for our purposes is a low formation temperature. The semiconducting silicides (Mn, Cr, Re, Fe, Ru) are not considered. The obtained resistivity, barrier height and formation temperature are strongly susceptible to variations in processing; values quoted in Table 2.1 are experimental results but should be considered approximate guides. In particular, some care is required to assign formation temperatures to specific silicide phases, as the progression through phases is a continuum.

2.2.4 Why nickel silicide?

The title of this chapter has already betrayed our selection of nickel silicide as a contacting process to investigate. Having now reviewed the requirements and options, we are in a position to justify this choice. As we have shown, there are several very different approaches to the problem of contacting buried dopant structures, and ideally we would not limit ourselves to only one. Indeed we have not - in parallel to the work described here, independent internal projects by other researchers have been carried out investigating the via technique, pre-doped contact regions and *in situ* electron microscope desorption. In this context, we are therefore in the position of selecting the optimal *silicide* for investigation. Following the preceding overview of silicide properties, we arrive at nickel by the following reasoning:

Table 2.1: **Properties of thin-film metallic silicides**

		Silicide			
Class	Metal	Barrier height to n-Si (eV)	Phase	Formation temp. (°C)	ρ (300 K) ($\mu\Omega$cm)
Near-noble	Cobalt	0.69[44]	Co_2Si	300[45]	70[45]
			CoSi	450[46]	147[47]
			$CoSi_2$[1]	600[46]	15[48]
	Nickel	0.66[44]	Ni_2Si	300[49]	24[47]
			NiSi	400[49]	10.5[47]
			$NiSi_2$	800[46]	34[48]
	Copper		Cu_3Si		53[47]
	Palladium	0.74[50]	Pd_2Si	470[49]	30[49]
	Iridium	0.94[50]	IrSi		
	Platinum	0.87[50]	Pt_2Si	265[49]	
			PtSi	400[49]	35[50]
Refractory	Titanium	0.58[44]	$TiSi_2$ (C49)	550[45]	60[45]
			$TiSi_2$ (C54)	700[45]	15[45]
	Vanadium	0.65[50]	VSi_2		55[50]
	Zirconium	0.55[50]	$ZrSi_2$		40[50]
	Niobium	0.65[44]	$NbSi_2$[2]		50[50]
	Molybdenum	0.55[50]	$MoSi_2$		100[50]
	Tantalum	0.59[50]	$TaSi_2$[3]		55[50]
	Tungsten	0.65[50]	WSi_2		70[50]
Rare earth	Lanthanum		$LaSi_2$	275[43]	350[47]
	Cerium		$CeSi_2$[4]	400[43]	408[47]
	Neodymium		$NdSi_2$[5]		349[47]
	Promethium		$PrSi_2$[6]		202[47]
	Gadolinium	0.38[44]	$GdSi_2$[7]	325[43]	263[47]
	Terbium		$TbSi_2$[8]		90[47]
	Dysprosium	0.38[44]	$DySi_2$[9]	350[43]	3020[47]
	Holmium	0.38[44]	$HoSi_2$[10]	375[43]	
	Erbium	0.38[44]	$ErSi_2$[11]	400[43]	30[47]
	Ytterbium		$YbSi_2$		50[47]
	Lutetium		$LuSi_2$		100[47]

[1] Superconducting below $T_C \approx 1$ K[47]
[2] Superconducting below T_C=130 mK[47]
[3] Superconducting below T_C=350 mK[47]
[4] Ferromagnetic below T_C=12 K[51]
[5] Antiferromagnetic below T_C=10 K[52]
[6] Ferromagnetic below T_C=11 K[52]
[7] Antiferromagnetic below T_N=26 K[52]
[8] Antiferromagnetic below T_N=32 K[51]
[9] Antiferromagnetic below T_N=17 K[51]
[10] Antiferromagnetic below T_N=20 K[51]
[11] Ferromagnetic below T_C=4.5 K[51]

1. Rare earth silicides should be avoided so as not to introduce magnetic material into the device and thereby exacerbate magnetic field hysteresis

2. Refractory silicides require higher than desirable annealing temperatures in order to initiate the silicon diffusion required for their formation. To preserve the integrity of carefully patterned dopants, these temperatures are not acceptable.

3. Of the near-noble metals the three top candidates are cobalt, nickel and platinum. As previously discussed, for our application of contacting highly doped regions the barrier height is not critical, but it is still indirectly relevant by way of contributing to the barrier width. We therefore give preference to cobalt or nickel which have silicide barrier heights of ≈0.68 eV to n-type silicon. As a subject of active research with a large body of literature and widespread industrial adoption, nickel silicide is the choice of Ohmic contact we have reached.

In the following section we will outline a complete process sequence for contacting buried dopant devices with nickel silicide, taking into consideration all of the requirements raised in the preceding discussion.

2.3 Developing a nickel silicide contact recipe

Having chosen nickel silicide as a replacement metallization, in this section we develop a process sequence compatible with STM dopant devices. We begin by reviewing nickel silicide fabrication studies from the literature. Based on the information obtained, we discuss the unforeseen problems encountered in our own process development, before finally distilling and analyzing a fully compatible nickel silicide contact recipe.

2.3.1 Making nickel silicide: lessons from the literature

The body of literature surrounding nickel silicide is substantial[‡] owing to its application in microelectronic manufacturing. To provide a starting point for our own recipe we briefly review relevant findings of this literature. Before we begin it will be helpful to define a consistent nomenclature. Nickel silicide can exist in many different phases (i.e.. Ni_xSi_y), and in this chapter when we refer to 'nickel silicide' we are not implying any particular phase. When we wish to reference a particular stoichiometry we will either use chemical notation ('NiSi') or explicitly specify the form we mean ('nickel monosilicide').

[‡] At the time of writing, a search on the Web of Knowledge database produces over 1400 articles. A useful starting point is the review article by Lavoie *et al*[42]

Though many different stoichiometric configurations of nickel silicide are stable at room temperature [§] in practice it is found that the predominant progression during annealing is:

$$\mathrm{Ni} + \mathrm{Si} \xrightarrow{heat} \mathrm{Ni}_x\mathrm{Si} \xrightarrow{heat} \mathrm{NiSi} \xrightarrow{heat} \mathrm{NiSi}_2$$

where x is > 1 (i.e. a metal rich phase). The progression of the reaction can be determined by monitoring sheet resistance, as illustrated in Figure 2.9. In this experiment the sheet resistance of a nickel-polysilicon bilayer was monitored continuously inside a furnace while the temperature was ramped; peaks and plateaus can be reliably assigned to different silicide phases (confirmed by x-ray diffraction studies). Metal rich silicide phases begin forming within 1-2 minutes at temperatures above 200°C[42]. This continues until temperatures beyond ≈ 320 °C, when all metal rich phases are converted to NiSi. Given sufficient time all of the unreacted Ni is consumed, the silicide ceases to grow thicker and a constant sheet resistance is attained. Further heating to >650 °C can have two different outcomes. One is that the NiSi consumes more of the underlying silicon and transforms to $NiSi_2$, the other is that the NiSi agglomerates. Which of the two occurs depends on the starting film thickness and the heating conditions[53], but both outcomes sharply increase the sheet resistance. These high temperature instabilities occur well beyond the temperature range we will use. The temperatures indicated by Figure 2.9 for the various phase transitions are in agreement with several other rapid thermal anneal studies[53;54;55;56]. Where longer period furnace annealing is used, the phase transitions occur at lower temperatures[56], purely owing to the increased time available for reaction.

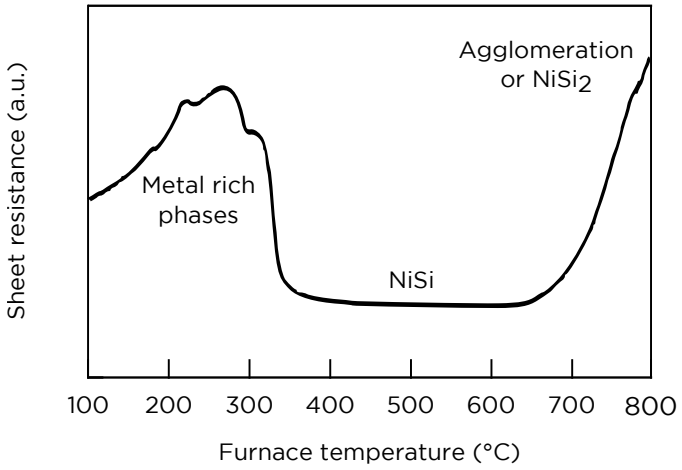

Figure 2.9: **Evolution of nickel silicide during annealing** A continuous measurement of the sheet resistance of a nickel-polysilicon bilayer during a furnace anneal, with the temperature ramping to 800°C over ≈ 5 minutes. The different stages of the silicide reaction can be determined by the changes in sheet resistance (*Adapted from Lavoie*[42]).

Transmission electron microscope (TEM) studies show that the planar silicide growth

[§] Six in fact: Ni_3Si, $Ni_{31}Si_{12}$, Ni_2Si, Ni_3Si2, NiSi and $NiSi_2$ [42]

front advances uniformly, as expected from diffusion limited growth. The depth of the silicide is hence a well defined quantity. Images from TEM also provide a direct measurement of silicide thickness, which closely reflects the stoichiometry - a 10nm film of nickel annealed at 450°C will react to form a self-limiting 22nm thick NiSi film after ≈30 s[54]. However the silicide grows both up and down (see Figure 2.10), so the *penetration depth* of the silicide is less than the silicide thickness, typically 82% of the total silicide thickness[57]. A 10nm film of nickel will hence create a silicide which penetrates 18 nm into the substrate. This penetration depth is reliable and self limiting, making silicides attractive where precise depth control is necessary. As nickel silicide formation is diffusion-controlled, growth proceeds as the square root of time:

$$d = \sqrt{\alpha t e^{\left(\frac{-E_A}{k_B T}\right)}}$$

where d is the silicide thickness, t the reaction time, T the reaction temperature, E_A the activation energy of the reaction and α an empirically determined prefactor. Experimental studies of nickel on silicon have found typical activation energies E_A=(1.5 - 1.7) eV and prefactors α=(0.7 - 1.5) cm^{2}s^{-1} [58;59;60], with some variation subject to the condition of the starting wafer and the specifics of the annealing equipment. To give an estimate of the time scales involve (taking the values obtained by Lien[60]) it would require ≈ 30 minutes to grow a 65nm film of NiSi at a furnace temperature of 300°C, and ≈ 3 minutes to grow the same thickness at 350°C.

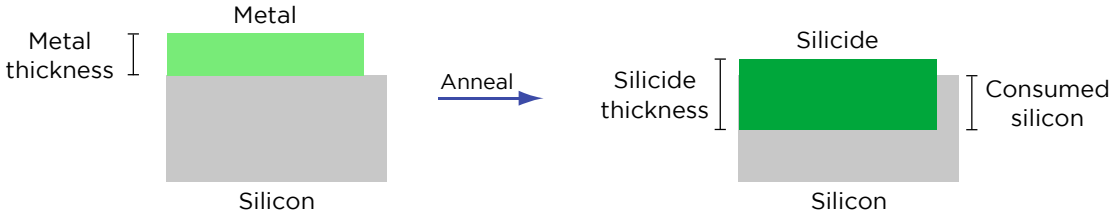

Figure 2.10: **Definition of terms for silicide thickness** A silicide film is thicker than its metal precursor, but grows primarily into the substrate.

A key reason for the industrial interest in nickel silicide is to avoid so-called *line width effects* where the resistivity of a material increases at small feature sizes. This typically arises in nucleation-controlled systems (nickel silicide is diffusion-controlled) due to a reduction in possible nucleation sites at small features. NiSi suffers no such effects at feature sizes as small as 30nm[53], however in certain circumstances nickel silicide encounters an *inverse* line width effect whereby the sheet resistance reduces at small feature sizes[53]. The inverse line width effect is unique to masked silicide reactions - i.e. where nickel is annealed as a continuous film on a barrier layer and silicidation only occurs in mask windows. It originates from excess nickel diffusing into the window, causing a thicker silicide film than intended. This is not a desirable behaviour - a more pessimistic as-

sessment is that depth control is lost at small feature sizes. For the work presented in this chapter we lift-off excess nickel *before* rather than after annealing, ensuring that the inverse line width effect cannot occur, hence obtaining reliable formation at all feature sizes.

In developing a nickel silicide process it is useful to know which chemical treatments can and cannot be tolerated. This will inform the design of cleaning and etching steps for the process. Extensive testing by Howell[61] showed that nickel silicide films are quite robust. Common cleaning solutions such as SP (H_2SO_4:H_2O_2), RCA1 (NH_4OH:H_2O_2:H_2O) and solvents such as IPA and acetone have no observable effect on the film morphology or sheet resistance. Solutions containing hydrochloric acid such as the RCA2 clean (HCl:H_2O_2) would occasionally but not consistently destroy nickel-rich films. Hydrofluoric acid (HF) creates an undetermined surface by-product, but this can be completely removed by simply rinsing the surface in deionized water after the HF treatment. Silicon etchants based on nitric acid completely removed the silicide, suggesting that metal etching solutions with similar chemistry (such as aqua regia) should be avoided.

We have discussed the fact that an oxide layer can mask silicidation. This can present a problem when an unintentional native oxide is present, slowing or preventing the silicide reaction. The native oxide can easily be removed with HF before nickel deposition, however it has been shown that this is not sufficient. Oxygen can diffuse through the nickel during silicidation, reaching and oxidizing the underlying silicon interface and slowing or stopping the silicidation reaction. A common solution is to include a thin titanium layer either as an interlayer (Si/Ti/Ni) or a cap (Si/Ni/Ti). As an interlayer the titanium can reduce the native oxide as well as getter oxygen from the nickel, but this comes at the expense of impeding the diffusion of nickel into the silicon by two orders of magnitude, pushing up the formation temperature by more than 100 °C[62]. In cases where such an increase in temperature is unacceptable, capping layers have shown similar native oxide reduction for both cobalt[63] and nickel silicidation[64], but only for thick capping layers and high annealing temperatures. Where no native oxide is present, the chief role of the capping layer is to protect the nickel from oxygen contamination. Both Wu[65] and Tan[64] noted the formation of high resistivity ternary Ni-Ti-Si compounds at the surface, which could not be removed by etching but could be avoided by using thin capping layers and low annealing temperatures. The indication is that a capping layer will be a necessary component of the contacting process we develop, but it is not clear *a priori* how detrimental the presence of a high-resistivity ternary layer would be.

2.3.2 Developing a nickel silicide process

From the results described in the preceding section, we can make the following observations about developing a contacting scheme for STM-patterned dopant devices:

- The starting nickel thickness should be at least half the depth of the buried dopant layer. Whilst in principle thicker starting layers can be used they will require longer annealing times to complete the silicide reaction (contrary to our desire to maintain the lowest possible thermal budget)
- 300°C for 30 minutes is a good starting point for the formation anneal to obtain the monosilicide phase, but variations of both temperature and time should be investigated to establish the minimum possible thermal budget.
- A titanium capping layer may be necessary to avoid silicon oxide formation (which hinders the silicide reaction). However we should also try omitting it in order to avoid the formation of complex, high resistivity ternary compounds

The process recipe developed in this chapter is described in Figure 2.13, but before explaining it we first discuss some of the experiments used to arrive at this final recipe.

2.3.2.1 Metallization sequence

The simplest silicidation process would be to evaporate nickel onto silicon and anneal it. Since we are concerned about magnetoresistance artifacts from magnetic impurities, a good standard practice would be to follow this with a selective metal etch to ensure any unreacted (ferromagnetic) nickel is removed. The SP solution (H_2SO_4:H_2O_2) etches elemental metals very rapidly but as noted earlier has no effect on nickel silicide[61], and is therefore a good starting point.

However early tests with this simple process sequence resulted in unreliable gold-ball wire bond adhesion. To resolve this we explored a number of variations, as summarized in Figure 2.11. Variations outlined in red did not result in successful bond adhesion, while those in green did. The results can be summarised as follows:

- Bonding directly to the silicide is not possible
- A thin Ti:Au adhesion layer deposited after silicidation was successful only if in addition a titanium cap was present on the nickel prior to the silicidation anneal.
- A single-step metallization using a very thick (100nm) gold layer on top of the nickel was partially successful; the bond would adhere to the film but the gold was poorly adherent to the silicide.

On this basis we used the Ti capping process for the silicidation anneal, followed by a Ti:Au adhesion layer. This gave a 100% success rate for the dozens of bonds subsequently made in this chapter. It is not clear why the Ti cap is necessary for bonding, and no literature exists on the bond-adhesion properties of nickel silicide films. We speculate that the mechanical properties of the thin Ni-Ti-Si ternary surface layer may be responsible for this bonding behaviour.

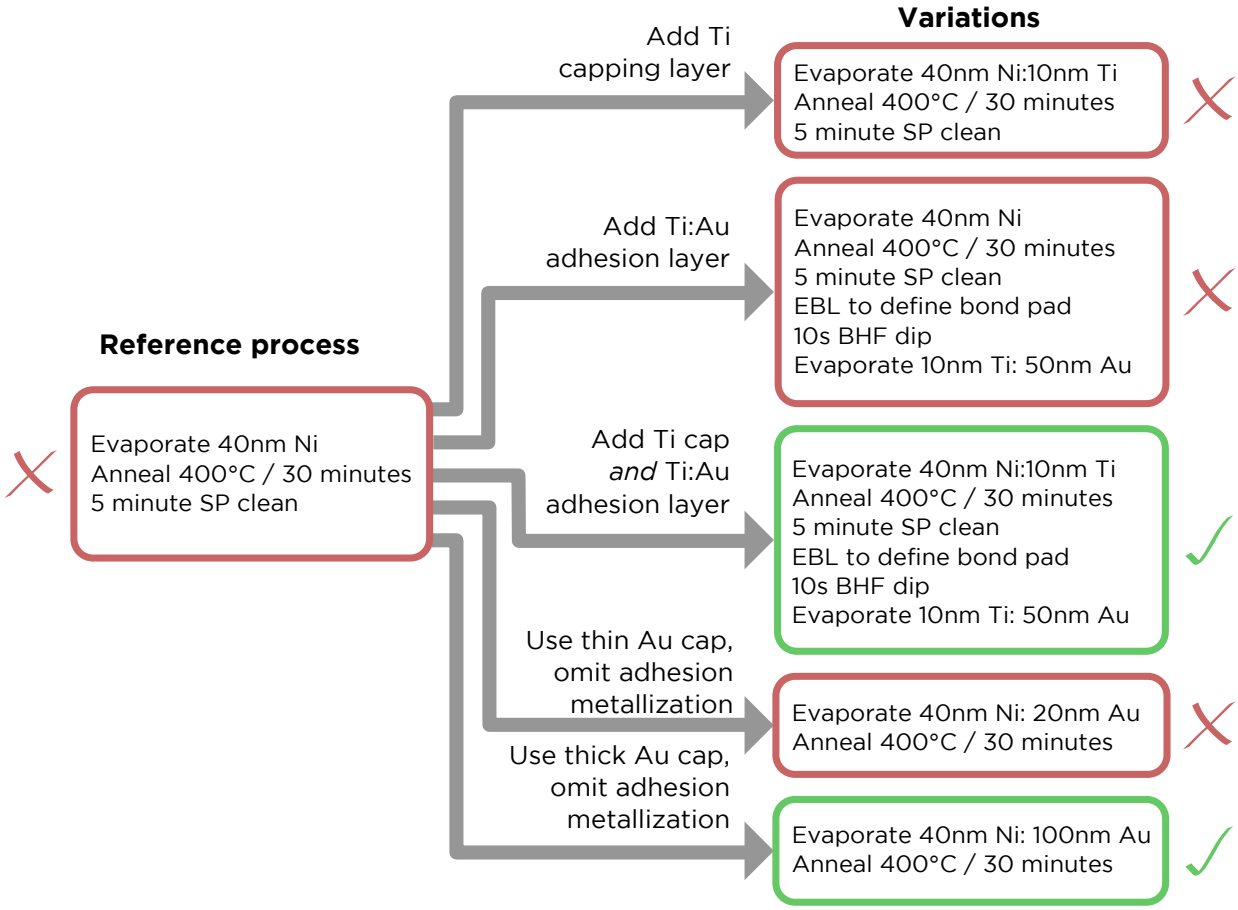

Figure 2.11: **Determining a functional process sequence for nickel silicide Ohmic contacts** An overview of the simplest silicide process (left) and the variations attempted (right). Red/green boxes indicate failure/success in making a gold-ball wire bond to the layer. (*BHF - buffered hydrofluoric acid. EBL - electron beam lithography*)

Table 2.2: **Monitoring the progression of the silicide reaction as a function of annealing temperature and time.**

Annealing temp. (°C)	Annealing time (minutes)	Sheet resistance ($\Omega/\square$)
250	30	3.7
300	30	2.2
350	30	2.2
400	30	2.2
300	5	5.0
300	20	2.7
300	30	2.2

2.3.2.2 Anneal conditions

We saw in Figure 2.9 that monitoring the sheet resistance of a silicide film is a useful technique for determining the silicidation progress. To determine an appropriate annealing temperature we performed a similar experiment, summarised in Table 2.2. To perform this we evaporated a 40 nm:10 nm Ni:Ti bilayer onto a 7 Ωcm n-type Si(100) wafer. This was then cleaved into several 1cm $\times$ 1cm sections, and the sections furnace annealed under a range of temperature/time conditions. We then measured the sheet resistance of these samples using a conventional 4 point probe system. The results of these measurements are recorded in Table 2.2.

The measurement results in Table 2.2 were performed at room temperature on a conductive substrate, such that the values shown do not represent the true sheet resistance of the silicide alone. However if the object is simply to monitor the progression of silicide phases then it is only the relative changes in sheet resistance which we need to know. In the first set of measurements we have varied the annealing temperature, and it is apparent that the sheet resistance has reached a plateau by 300°C. This is in good agreement with Figure 2.9, and confirms that 300°C is the lowest value we should use to obtain the monosilicide phase. In the second set of data we have fixed the annealing temperature at 300°C but varied the annealing time from 5 to 30 minutes. These samples do not reach the same limiting value of sheet resistance corresponding to complete monosilicide formation without the full 30 minute anneal. We can therefore conclude that for these 40nm thick films an annealing condition of 300°C for 30 minutes is optimal.

2.3.3 Final NiSi fabrication recipe with example

The final aim of this chapter is to develop an alternative Ohmic contact for STM-patterned dopant devices. However this requires a large throughput of samples, and STM-patterned devices are time consuming to create. As a consequence, for this chapter we instead

use uniformly δ-doped Si:P samples, grown under identical conditions to those of STM-patterned devices. These samples are then mesa etched *ex situ* to define a Hall bar, as shown in Figure 2.12. All of the important steps in the metallization are unchanged between Hall bar and device processing. Hall bar samples also provide a straightforward means of extracting material properties of the δ-layer such as the carrier density, mobility and phase coherence length, enabling us to determine whether the new process has caused any unintended alteration of these properties.

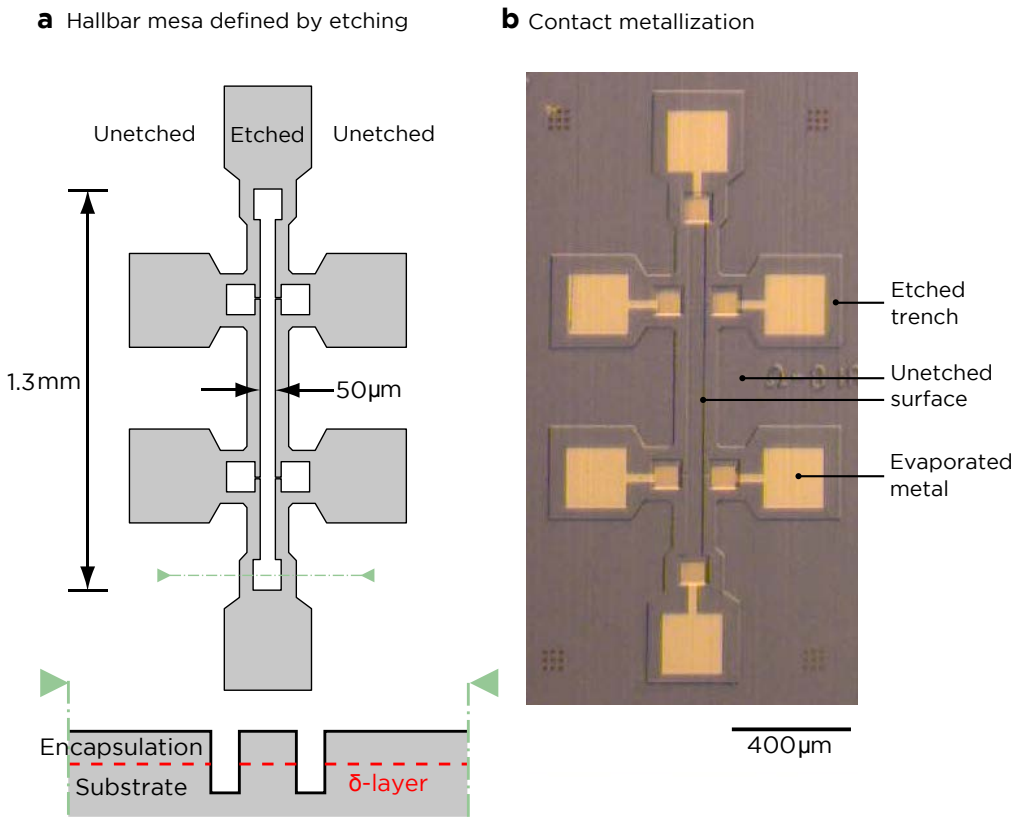

Figure 2.12: **Details of the Hall bar structure.** In this chapter we use Si:P δ-doped samples without STM patterning, using *ex situ* mesa-etching to isolate Hall bar patterns for subsequence analysis (a). The optical microscope image (b) shows a sample after completing metallization but prior to wire bonding.

In Figure 2.13 we outline an example process flow for creating nickel silicide contacts to a δ-doped Si:P Hall bar structure. Figure 2.13 should be read as a sequence from top to bottom. The first section covers the process of mesa-etching the Hall bar structure of Figure 2.12a. The next section contains the nickel silicide metallization process based on the work of the preceding sections, and shown completed in Figure 2.12b. The final section covers the packaging and bonding process to enable electrical measurements. For the purposes of comparison, in Figure 2.14 we indicate the process flow for making aluminium contacts.

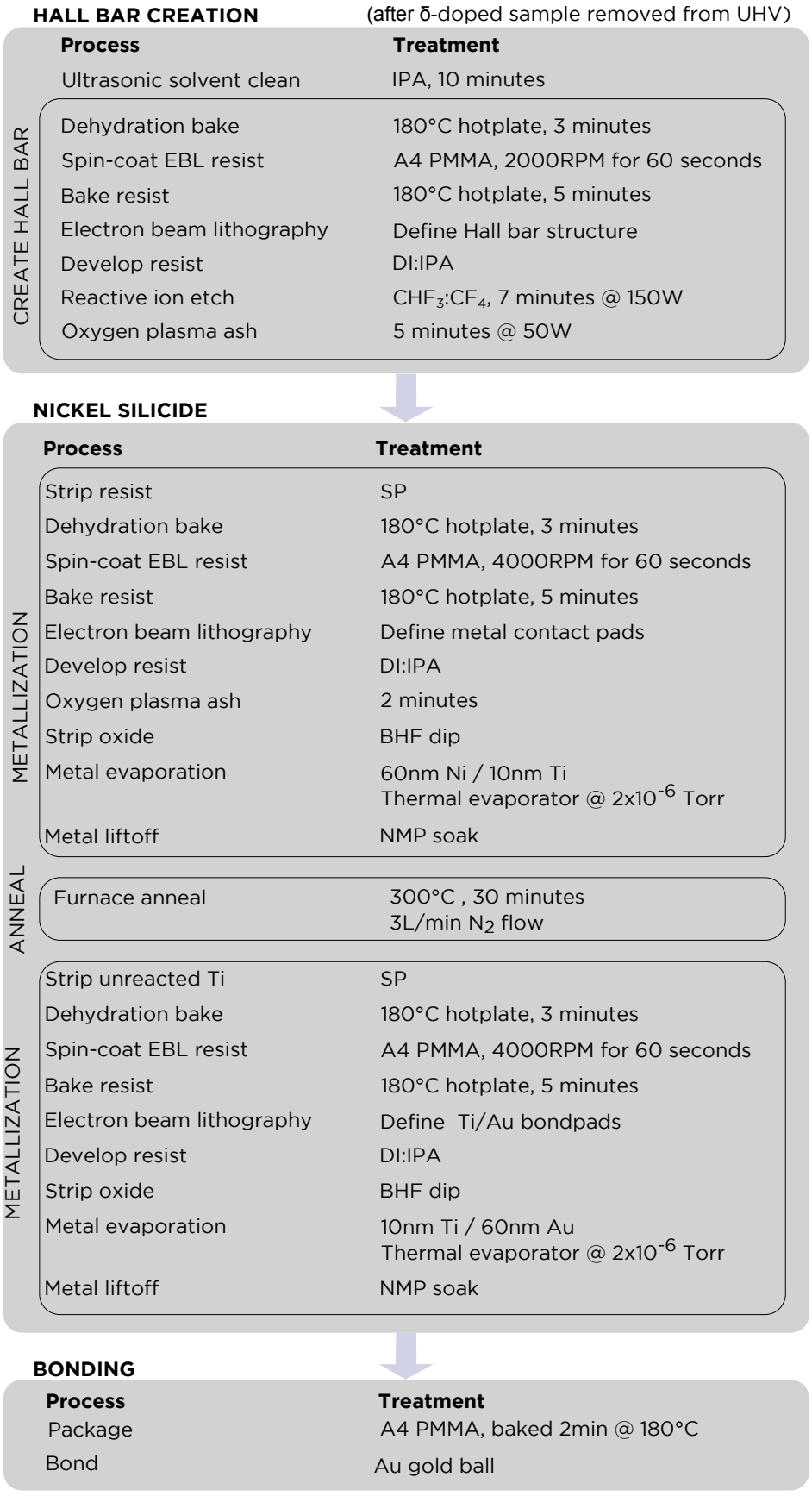

Figure 2.13: **Process sequence for a nickel silicide contacted Hall bar**

HALL BAR CREATION (after δ-doped sample removed from UHV)

	Process	Treatment
	Ultrasonic solvent clean	IPA, 10 minutes
CREATE HALL BAR	Dehydration bake	180°C hotplate, 3 minutes
	Spin-coat EBL resist	A4 PMMA, 2000RPM for 60 seconds
	Bake resist	180°C hotplate, 5 minutes
	Electron beam lithography	Define Hall bar structure
	Develop resist	DI:IPA
	Reactive ion etch	CHF_3:CF_4, 7 minutes @ 150W
	Oxygen plasma ash	5 minutes @ 50W

ALUMINIUM

	Process	Treatment
	Strip resist	SP
METALLIZATION	Dehydration bake	180°C hotplate, 3 minutes
	Spin-coat EBL resist	A4 PMMA, 4000RPM for 60 seconds
	Bake resist	180°C hotplate, 5 minutes
	Electron beam lithography	Define metal contact pads
	Develop resist	DI:IPA
	Oxygen plasma ash	2 minutes
	Strip oxide	BHF dip
	Metal evaporation	80nm Al Thermal evaporator @ $2x10^{-6}$ Torr
	Metal liftoff	NMP soak
ANNEAL	Furnace anneal	350°C , 30 minutes 3L/min N_2 flow

BONDING

Process	Treatment
Package	A4 PMMA, baked 2min @ 180°C
Bond	Au gold ball

CHEMICAL TREATMENTS:

Abbreviation	Chemicals	Mixing ratio	Time
SP	H_2SO_4:H_2O_2 H_20	3:1	10 minutes 10 minutes
DI:IPA (ultrasonic)	H_20: IPA	3:7	45 seconds
BHF dip	HF:H_2O:NH_4F H_20		10 seconds 1 minute
NMP soak	(N-methyl-2-pyrrolidone)		>3 hours

Figure 2.14: **Process sequence for an aluminium contacted Hall bar**

We make comments on specific steps in the nickel silicide process as follows:

- An oxygen plasma ash and buffered HF dip is performed immediately before the nickel evaporation to ensure a clean interface for the silicide reaction
- The 60nm nickel thickness is more than required to contact a typical $\approx$ 30nm deep buried dopant layer, but is used here to ensure that a continuous film is formed up the sidewalls of the Hall bar mesa.
- For patterned metallizations it becomes possible to confirm that a silicide reaction has occurred by simply measuring the height profile of the metal before and after annealing. Based on our previous discussion we would expect 60 nm of nickel to create $\approx$130 nm of NiSi, of which $\approx$24 nm will protrude from the surface. Assuming the 10nm Ti cap remains unchanged, we therefore expect a post-anneal height of $\approx$34 nm. This agrees with the measured height change based on stylus profilometer measurements, shown in Figure 2.15.
- An SP etch after the anneal guarantees no elemental nickel or titanium metal remains on the sample.
- The buffered HF dip prior to the Ti:Au evaporation is crucial, as silicides grow a native oxide at similar rates to bare silicon[66]

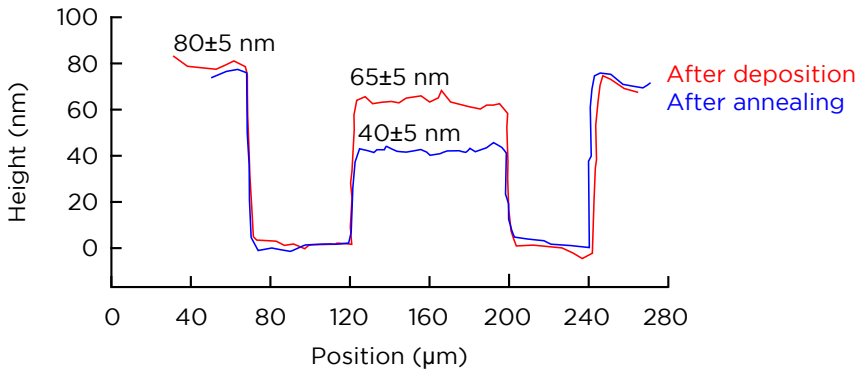

Figure 2.15: **Evidence of a silicidation reaction** Stylus profilometer traces of a Ni:Ti feature before (blue) and after (red) annealing. The 70nm tall (60nm Ni + 10nm Ti) feature has shrunk to 40nm after annealing, consistent with a silicide reaction into the substrate.

2.4 Comparative electrical characterization study of Al and NiSi contacts

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Having developed a nickel silicide contact recipe compatible with STM-patterned devices, in this section we evaluate the performance of these contacts at low temperature. We first discuss the measurement methodology and the use of Hall-effect and weak localization measurements. Next we demonstrate that Ohmic contact is successfully made to the δ-layer at low temperature, and estimate the contact resistance. Through the use of magnetotransport measurements we demonstrate that using nickel silicide has not influenced the phase coherence in the δ-doped system. Finally we investigate the measurement artifacts discussed in section 2.1, and show that the use of nickel silicide successfully eliminates the superconductivity artifact without influencing the dynamic hysteresis artifact.

2.4.1 Methodology and initial characterization

In the preceding section we focused on fabrication concerns for integrating nickel silicide. Ultimately our concern is whether nickel silicide outperforms aluminium in low-temperature magnetoresistance studies. To facilitate a direct comparison we fabricated a Si:P δ-doped sample, cleaved it in half and used these halves to fabricate Hall bars for a comparative study.

Closely following the fabrication method outlined in section 2.1, a 1-10 Ωcm n-type Si(100) substrate was annealed to 1100°C in UHV by direct current heating to produce a 2×1 surface reconstruction. The surface was then δ-doped by saturation dosing with 1.1 Langmuir of PH_3 gas at room temperature, followed by a 350°C anneal to incorporate the phosphorus into the silicon lattice. After encapsulating with 30nm of epitaxial silicon at a sample temperature of 250°C, the sample was removed from UHV for Hall bar processing.

For a comparative study, the original sample was split in half and Hall bar samples with nickel silicide (Figure 2.13) and aluminium (Figure 2.14) were created. Two Hall bars were created with each metallization, for a total of four Hall bars. We note one important diversion from the nickel silicide process described in Figure 2.13: the furnace annealing temperature was increased by 50 °C to 350°C in order to match the aluminium process. This was done to ensure that the condition of the δ-layer for the two samples was as identical as possible.

Initial DC characterization of these samples at 4.2 K showed all contacts were Ohmic (Figure 2.16). At this temperature the weakly doped substrate is no longer conductive due to incomplete dopant ionization, so Ohmic transport indicates successful contact to

the degenerately doped two-dimensional electron gas (2DEG) from the δ-doping layer.

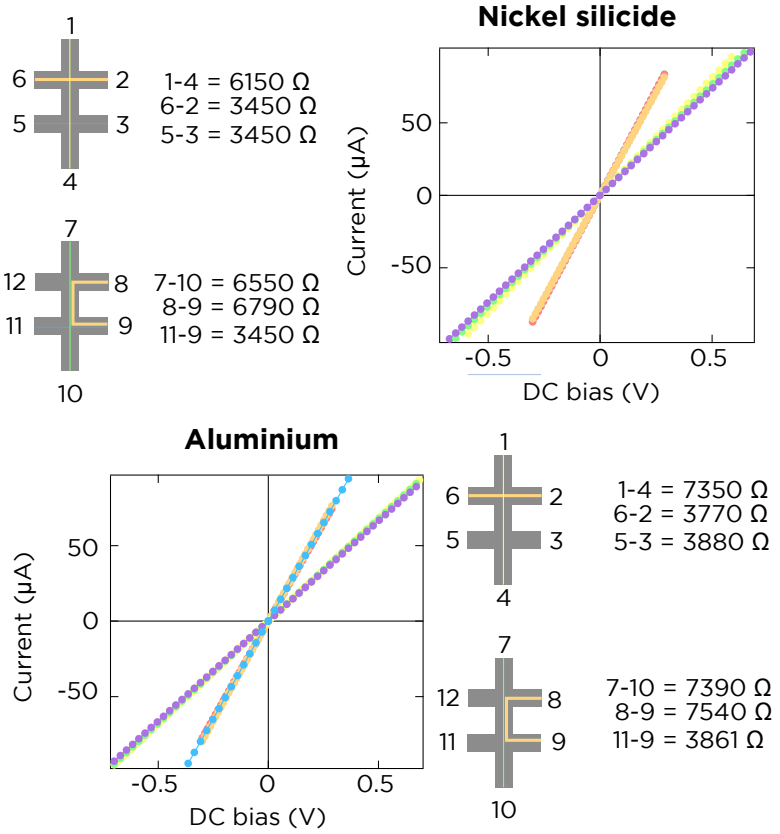


Figure 2.16: **Verifying Ohmic contact to the δ-doped layer** Two terminal DC current-voltage traces at 4 K confirm that all contacts are Ohmic.

Hall effect measurements are a convenient method of measuring the carrier density in the δ-layers. By applying a perpendicular magnetic field B to a current-carrying δ-layer we induce a potential transverse to the direction of current flow. Relating this potential to the source-drain current we can define a Hall magnetoresistance $R_{XY}(B) = V_{XY}/I_{SD}$ (see Figure 2.17), which has the well known property:

$$\frac{dR_{XY}}{dB} = -\frac{1}{ne}$$

with B the perpendicular magnetic field and n the carrier density. By measuring the Hall resistance as a function of the applied magnetic field we can determine the carrier density in the 2DEG. Such measurements at a temperature of 4 K yield carrier densities of $(1.36 \pm 0.01)\times10^{14}$ cm^{-2} and $(1.51 \pm 0.02)\times10^{14}$ cm^{-2} for the aluminium and nickel Hall bar respectively. A variation of $\pm$ 5% is not unreasonable across a sample (due to a spatially varying temperature profile during the flash anneal).

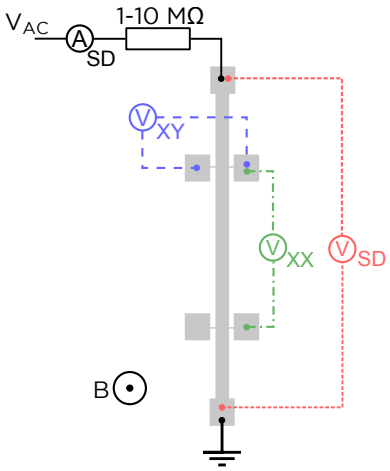


Figure 2.17: **Hall bar measurement configuration** The circuit diagram for constant-current AC magnetoresistance measurements with a Hall bar structure. With a maximum Hall bar resistance of <10 kΩ, the MΩ series resistor serves to maintain a constant current. Lock-in amplifiers (10 MΩ input impedance) provide the AC excitation and sense the labeled voltages and current.

2.4.2 Extracting the Ohmic contact resistance

A Hall bar structure does not permit direct measurement of the metal-semiconductor contact resistance, but from a comparison of two- and four-terminal resistances combined with knowledge of the geometry of the Hall bar, we can obtain an upper bound. To achieve this we simultaneously measure the two-terminal resistance $R_{SD} = \frac{V_{SD}}{I_{SD}}$ and four-terminal resistance $R_{XX} = \frac{V_{XX}}{I_{SD}}$ of the sample using low frequency AC (see Figure 2.17). This is performed with no applied magnetic field and at a temperature of 4 K, which is sufficiently cold that the substrate does not conduct but not yet cold enough for superconductivity artifacts to manifest. The Hall bar was designed to have a channel length-to-width ratio of precisely 12, which means the four-terminal measurement encompasses 12 'squares' of the δ-doped layer. By counting squares we can put a bound on the size of the entire Hall bar of 23 to 24 squares (see Figure 2.18), an uncertainty of ≈2%. Comparable uncertainty could potentially arise from the calibration of the voltage and current measurement instruments, but for now we assume this to be negligible, seeking only an estimate of the total contact resistance (source + drain) of the Hall bar:

$$R_C = R_{SD} - \frac{23.5 \pm 0.5}{12} R_{XX}$$

The results of these calculations are summarized in Table 2.3. We see that the contact resistance for the nickel silicide Hall bars is *at most* 130 Ω (or 65 Ω per contact), and as expected is not significantly different to that of the aluminium contacted Hall bars at 132 Ω. This contact resistance is much smaller than the ≈ 7 kΩ resistance of the Hall bar itself.

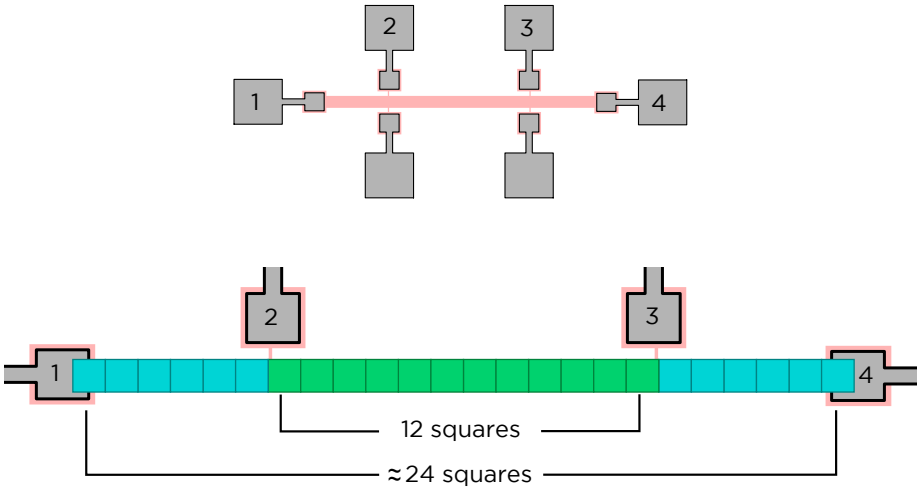


Figure 2.18: **Estimating contact resistance from Hall bar geometry** Two terminal resistances are composed mainly of the resistance from the δ-doped channel and the metallization contact resistance. By counting the number of squares in the Hall bar structure we can approximately separate the two contributions.

Sample	R_{XX} (Ω)	Measured R_{SD} (Ω)	Predicted R_{SD} (Ω)	**Maximum total R_C (Ω)**
Aluminium HB1	3829	7459	7339 - 7658	**120**
Aluminium HB2	3843	7498	7366 - 7686	**132**
Nickel silicide HB1	3566	6906	6835 - 7132	**71**
Nickel silicide HB2	3430	6704	6574 - 6860	**130**

Table 2.3: **Estimating contact resistance for the Hall bars**. An estimation of the total contact resistance (source + drain) of the Hall bars studied here. The predicted R_{SD} corresponds to the source-drain resistance of the δ-doped Hall bar with zero contact resistance, using estimated geometries of 23 to 24 squares. Maximum R_C values are taken as the difference between the measured R_{SD} value and the lowest possible predicted R_{SD}.

2.4.3 The impact of metallization on electrical transport properties

Since our interest lies in investigating artifacts during quantum transport measurements, subsequent milliKelvin temperature measurements were performed in a dilution refrigerator that allowed simultaneous measurement of both samples with perpendicular fields up to 8 T. Magneto-transport measurements were performed using standard low-frequency (17 Hz) lock-in techniques with a 5 nA constant current. It is important to determine whether the use of nickel silicide has impacted transport behaviour in the δ-layer, and also whether we have impacted the thermal equilibration of carriers. Both of these questions can be addressed by examining the zero field conductivity of the δ-layer as a function of temperature.

Electron transport in such highly doped 2D layers is highly diffusive, as the carriers are confined to the same spatial plane as the ionized donors. The total conductivity can be considered in terms of a classical Drude conductivity σ_D with modifications $\delta\sigma_{WL}$ and $\delta\sigma_{EEI}$ due to *weak localization* and *electron-electron interactions*[67] :

$$\sigma(B,T) = \sigma_D + \delta\sigma_{WL}(B,T) + \delta\sigma_{EEI}(T)$$

The weak localization contribution stems from electrons becoming locked into phase coherent scattering loops[68], where each loop represents an electron staying spatially localized instead of contributing to conduction:

$$\delta\sigma_{WL}(B,T) = \alpha\frac{e^2}{\pi h}\left[\Psi\left(\frac{1}{2}+\frac{B_\phi(T)}{B}\right) - \Psi\left(\frac{1}{2}+\frac{B_0(T)}{B}\right) + \ln\frac{B_0(T)}{B_\phi(T)}\right]$$

with T the system temperature, α a phenomenological prefactor relating to intervalley scattering, B the applied magnetic field and B_ϕ and B_0 characteristic magnetic field values deriving from the electron phase relaxation time τ_ϕ and transport relaxation time τ_e. The coherent scattering loops can be disrupted by the application of a magnetic field, giving rise to a negative magnetoresistance characteristic of highly diffusive systems (Figure 2.19a).

The electron-electron interaction describes the scattering of electrons from the electromagnetic background of the other electrons (similar to the familiar electron-phonon interaction), and is described by[69]:

$$\delta\sigma_{EEI}(T) = K_{ee}\frac{e^2}{\pi h}\ln\left(\frac{kT\tau_e(T)}{\hbar}\right)$$

with K_{ee} a parameter relating to the strength of the Coulomb interaction. At zero magnetic field the weak localization term can be simplified, resulting in a modified expression for the conductivity:

$$\sigma(B=0,T) = \sigma_D + \alpha\frac{e^2}{\pi h}\ln\left[\frac{\tau_e}{\tau_\phi}\right] + K_{ee}\frac{e^2}{\pi h}\ln\left[\frac{kT\tau_e(T)}{\hbar}\right]$$

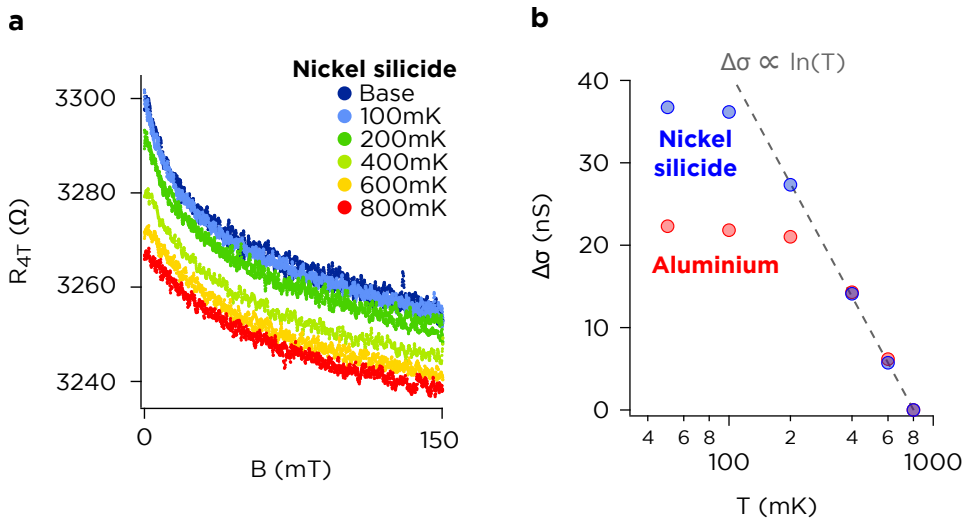


Figure 2.19: **Comparison of electrical transport for an aluminium and nickel silicide contacted Si:P δ-layer.** Temperature dependent four-terminal magnetoresistance measurements of the Hall bar samples (as shown for the nickel silicide sample in (a)) reveal quantum conductivity corrections. Analysis of the temperature dependent zero-field conductivity for both samples (b) indicates no difference in the quantum transport behaviour, but differing limiting temperatures.

In disordered 2D systems at low temperatures (as is the case here) the electron phase coherence is dominated by Nyquist scattering, leading to a $1/T$ dependence for τ_ϕ. This leads to a $\ln(T)$ dependence for both the weak localization and electron-electron interaction corrections, allowing further simplification of the zero-field conductivity:

$$\sigma(B=0,T) = \sigma_D + \gamma \ln(T) \tag{2.1}$$

where we have collected all of the quantum correction parameters into a single parameter γ. In Figure 2.19b for both the aluminium and nickel silicide Hall bars we plot the quantity $\Delta\sigma$, which is the change in the zero field conductivity from the value at 800 mK:

$$\Delta\sigma = \sigma(B=0,T) - \sigma(B=0,T=800\text{mK})$$

It is clear from this figure that the temperature dependence does indeed proceed with the $\ln(T)$ dependence predicted from Equation 2.1 until the electron temperature saturates between 100-200 mK. Importantly, both samples have the same γ, indicating that the different contact processes have had no influence on the quantum transport properties of the δ-layer. We can also see from Figure 2.19b that the two samples have different limiting electron temperatures, with the nickel silicide sample saturating at $\approx$100 mK compared to $\approx$200 mK for the aluminium sample. This can readily be explained by the lower Drude conductivity of the aluminium sample, a consequence of the lower active carrier density compared to the nickel silicide sample (1.36 vs. 1.51)$\times 10^{14}$ cm^{-2}. This

results in a larger joule heating power ($P = I^2R$) and therefore a higher limiting temperature. This variation in carrier density across the two samples is, again, easily explained by non-uniform heating of the samples during *in situ* preparation. It is clear however that the use of nickel silicide contacts is not negatively impacting the thermal equilibration of carriers.

2.4.4 Understanding and eliminating superconductivity artifacts

We have previously alluded to a measurement artifact arising from the use of superconducting aluminium contacts. In this section we will confirm that it is absent with the nickel silicide contacting scheme, and then use the aluminium sample to characterize and explain the artifact.

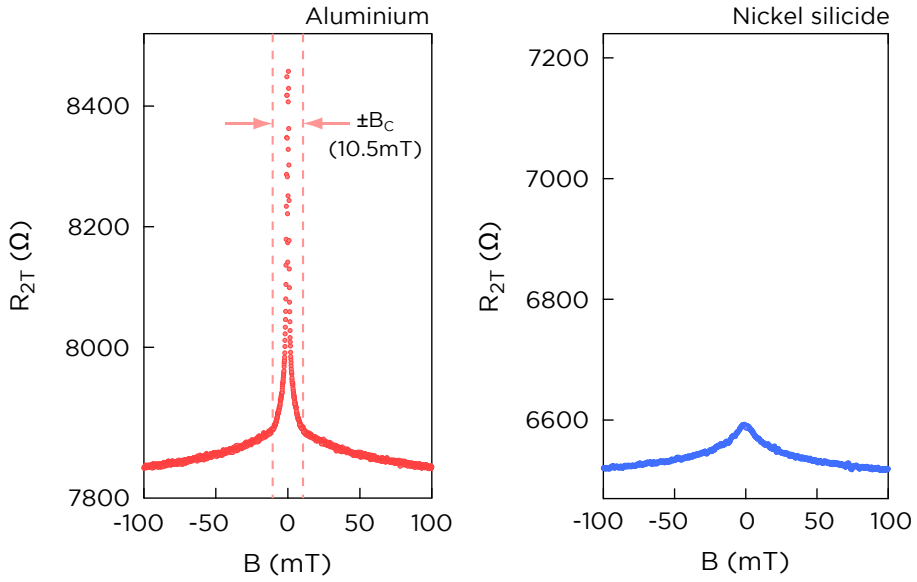


Figure 2.20: **Anomalous magnetoresistance peak due to aluminium contacts at milliKelvin temperatures.** A sharp resistance peak appears in two-terminal measurements of an aluminium contacted Hall bar, within a field range commensurate with the critical BCS field for aluminium of ± 10.5mT[70]. The resistance spike is absent in the nickel silicide contacted Hall bar.

The peak in contact resistance due to superconducting aluminium contacts can be seen in two-terminal magnetoresistance measurements such as those shown in Figure 2.20. Here we have measured the two-terminal resistance at the base temperature of the dilution refrigerator (nominally 50 mK) over a range of ± 100 mT. At first glance it may seem counterintuitive that we obtain a resistance *increase* from superconducting contacts. To explain this behaviour it will first be necessary to briefly review basic properties of type I (i.e. elemental) superconductors. Superconducting metals display several unusual properties compared to their normal-state equivalents. The most obvious of these is an abrupt disappearance of electron-phonon scattering events (and hence electrical resis-

tivity) below a certain critical temperature T_C. The physical origin of this behaviour is explained by the microscopic theory of Bardeen, Cooper and Schrieffer (BCS)[71]. Cooper had earlier shown that the second-order attractive electron-phonon interaction, while weak, can nonetheless be sufficient to render a degenerate electron gas unstable against the formation of bound electron pairs[72]. A minimum amount of energy is required to break apart these pairs, which forms the basis of the BCS energy gap Δ.

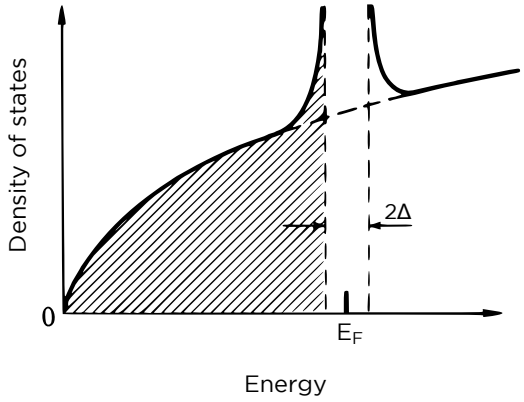


Figure 2.21: **BCS gap in the density of states** A schematic illustrating the influence of cooper pair formation on the 3D density of states in a bulk metal. Within a range 2Δ of the Fermi level the density of states is now zero, but is sharply peaked just beyond this range. (*Adapted from Burns*[32])

The property of most importance to the present discussion is the role of this energy gap on the density of states. One of the corollaries of BCS theory is a modification of the density of states in the 3D electron gas from the familiar $g(E) \propto \sqrt{E}$ to $g(E) \propto \frac{E}{\sqrt{(E-E_F)^2-\Delta^2}}$. As shown in Figure 2.21 the density of states is now zero within an energy range of 2Δ centered at the Fermi level; this is compensated by peaks on either side of this gap[¶] .

Figure 2.22 indicates the effect of this gap on electrical transport behaviour, first studied by Giaver and Megerle in 1961[73]. If we couple two normal-state metals tunnel through a thin insulating film[‖], a bias voltage applied across the two metals will result in Ohmic conduction (current proportional to applied voltage). When one of the metals enters a superconducting state, the transport behaviour is very different owing to the altered density of states. In the zero-temperature limit, no current can flow until the applied bias exceeds Δ. However the subsequent peak in the density of states results in a rapid increase in current, asymptotically approaching conventional metal-metal current-voltage

[¶]The gap in the density of states of is equal to twice the BCS gap of Δ. Where it is not clear from the context which gap is being referred to, the gap in the density of states is commonly referred to as the *spectroscopic gap*

[‖]The use of a thin insulating film here recognizes that realistic material junctions are seldom perfect. Some manner of barrier layer such as a surface oxide is likely to present, but with careful processing it can be so thin that tunneling is the dominant current transport mechanism and Ohmic conduction prevails

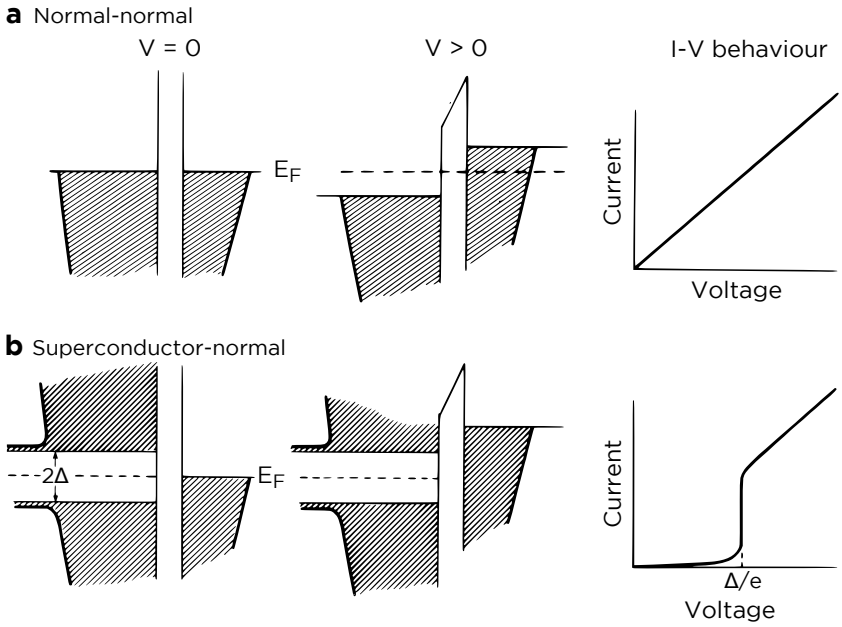


Figure 2.22: **Metal-metal and superconductor-metal contacts.** A schematic illustrating the origin of nonlinear current-voltage behaviour in superconductor-normal contacts. In the case of a metal-metal junction (a) the density of states is effectively constant; with ample states for carriers to move into the current scales in proportion to the applied bias. In a superconductor-metal junction (b) there are no states available until the applied bias exceeds the BCS energy gap Δ. (*Adapted from Burns*[32])

behaviour as the applied bias is increased further. Finite temperatures act to smear out the current-voltage behaviour, as thermal broadening of the Fermi occupation function makes a finite number of carriers available for transport even within the energy gap (indicated in Figure 2.22).

The rapid 'turn-on' behaviour of such a structure at biases equal to the energy gap led to practical applications as extremely sensitive radiation detectors[74]. However it is the blockaded sub-gap region which is relevant to the present discussion. A metal to δ-doped semiconductor contact is essentially identical to tunnel-coupled metal-metal contacts. The doping in the semiconductor is sufficiently high that tunneling through the Schottky barrier is the dominant current transport mechanism. Considering our aluminium contacts, we thus expect a region of blockaded transport for applied biases less than the BCS gap:

$$\begin{aligned} \Delta(T=0) &= 1.76kT_C \\ &= 177\mu\text{eV} \end{aligned}$$

Where we have used a critical temperature of 1.17K for aluminium[32]. The highest two

terminal resistance we see in this Hall bar is ≈ 8.5 kΩ, and the highest measurement current used is 5 nA. We therefore expect a maximum potential difference of 42 μV across *the entire Hall bar device*. Even in a hypothetical limit where the contact resistance dominates the entire device, the bias across each contact would not exceed $\approx$21 μV, far lower than the 177 μV required to resume regular conduction. We are thus limited to conduction by carriers thermally excited above the BCS gap. We can confirm this by examining the temperature dependence of the resistance peak (Figure 2.23. As a thermally activated process we should see an exponential increase in resistance as the temperature in the dilution refrigerator is reduced. The inset of Figure 2.23 shows that this is indeed the case until the electron temperature saturates below 200 mK. BCS theory also predicts a critical magnetic field at which superconductivity is eliminated, which for aluminium is $\pm$10.5 mT[70]. This is in good agreement with the onset of the resistance peak in our magneto-transport measurements, as indicated in Figure 2.20.

We now fully understand the origin of the superconductivity artifact in magneto-transport measurements. It is clear that when using superconducting contacts to measure sensitive quantum electronic devices it is impossible to avoid this effect. It is hence an important result that we are able to eliminate it through the use of the new nickel silicide contacting process.

2.4.5 Comparing the magnitude of hysteresis in magnetotransport

The second measurement artifact which we wish to avoid is the rate dependent occurrence of magnetic-field hysteresis. Such hysteresis can arise from a number of sources (such as eddy current heating, adiabatic demagnetization or residual magnetization), but in all cases the effect is to alter the shape of magnetoresistance traces. Since we rely on fitting curves to low field magnetoresistance traces in order to extract the phase coherence length, it is essential that they are not distorted by hysteresis artifacts. Since we see hysteresis in aluminium contacted samples (which are completely free of magnetic material), it is likely that the hysteresis originates from elsewhere in the cryostat such as the chip carrier package or cryostat sample socket. But considering that we are now using a ferromagnetic material (nickel) as a silicide precursor, it is important to investigate whether the hysteresis has been altered or enhanced. The electronic configuration of an elemental metal changes when the metal reacts to form a silicide. Hence whilst elements such as iron and nickel are magnetic as a pure metal, density functional theory calculations show that their silicides are non-magnetic[75]. Experimental confirmation of this is absent in the literature, with one study finding anomalies in the low temperature specific heat of NiSi which could be attributable to magnetic effects[76]. This reinforces the need for our own investigation into the hysteresis effect.

In Figure 2.24 we show the results of a comparative study of the hysteresis, measuring the longitudinal Hall bar magnetoresistance at sweep rates of the magnetic field from 200 to 10 mT/min. As the hysteresis is dynamic, such measurements indicate the magnitude

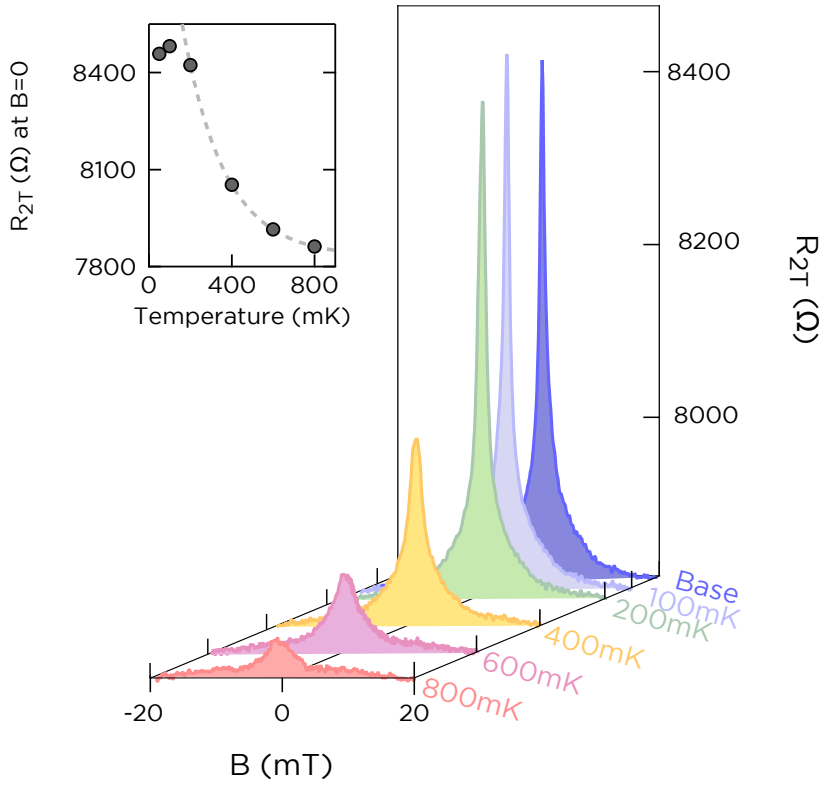


Figure 2.23: **Temperature dependence of the anomalous resistance peak** Measurements of the two-terminal magnetoresistance for the aluminium contacted Hall bar from base temperature to 800 mK. The inset illustrates the exponential increase in the magnitude of the resistance peak, suggestive of thermal activation over the BCS energy gap. The saturation of the peak below 20 0mK agrees well with Figure 2.19.

of the hysteresis and also the sweep rates required to avoid it. These measurements are all performed at the cryostat base temperature ($\approx$ 100mK), but the superconducting spike is no longer visible as this is a four terminal measurement which excludes contact resistance. The hysteresis in these measurements is very clear, and in some cases still persists at the slowest sweep rates of 10 mT/min, when an up-down sweep as shown takes 8 hours to complete.

Examining Figure 2.24a it is apparent that the hysteresis is stronger for the nickel silicide measurements. While the hysteresis is gone from the aluminium measurements at a sweep rate of 50 mT/min, for the nickel silicide we must go to 10mT/min. In order to test whether this is truly a characteristic of the nickel silicide sample, we swapped the two samples as schematically depicted in Figure 2.24b. The two samples were removed from the cryostat, and their chip packages swapped (which involved removing and remaking the wire-bonds). Repeating the hysteresis measurements in this new configuration as shown in Figure 2.24c**, it is clear that the hysteresis behaviour has reversed. The nickel

**The measurement filtering and integration time settings were not identical between the first and second measurement set, leading to a higher noise background in the second set

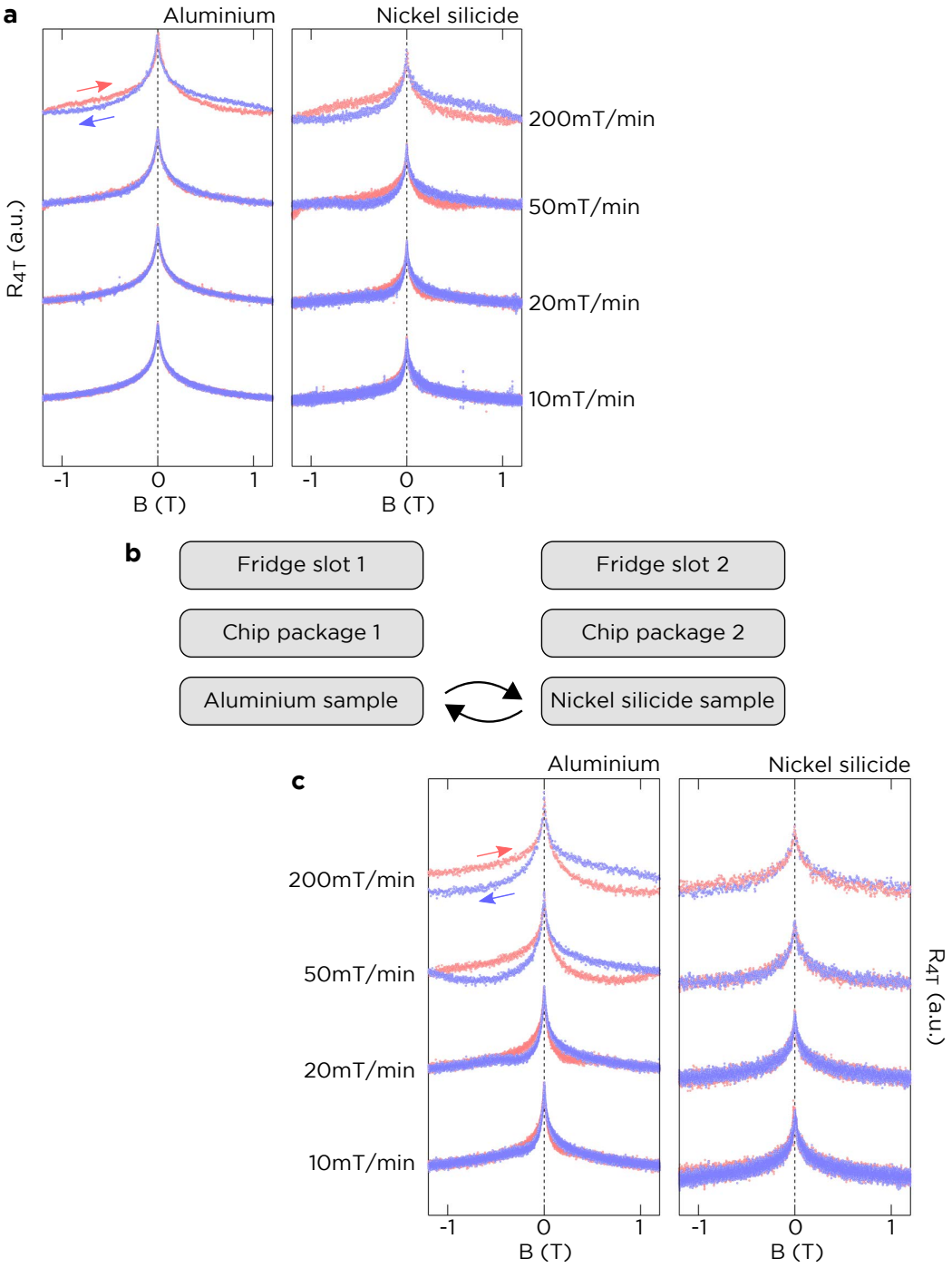


Figure 2.24: **An investigation of rate dependent magnetic field hysteresis.** Four terminal longitudinal Hall bar measurements of the aluminium and nickel silicide contacted samples, measured simultaneously (a). The direction and rate of the magnetic field sweeps are indicated. For rigor, we then swapped the two samples and repeated the measurements (b). The hysteresis does not correlate with the contact type, hence must originate from the chip package or cryostat position.

silicide sample is now hysteresis free at a sweep rate of 50 mT/min, while the aluminium sample continues to suffer hysteresis even at the slowest sweep rate of 10 mT/min. From this set of measurements it becomes clear that the strength of the dynamic hysteresis is not correlated with the contact metallization. We can conclude that the hysteresis instead originates from either the chip packages or the different sample holders within the cryostat. Importantly, the use of nickel silicide has in no measurable way increased the strength of the hysteresis.

Nonetheless, it is important to understand the origin of this hysteresis for future characterization work. On the basis of trends observed in Figure 2.24 we can comment on what mechanisms can be eliminated and deduced. That it is *dynamic* hysteresis eliminates joule heating (from excessive measurement currents) as a possibility, since this should depend only on the instantaneous device resistance. From careful examination of the peak shapes it can be seen that the magnetoresistance only deviates from the true, steady-state value when the applied magnetic field moves away from zero. This is very clear when overlaying traces, but can be also be seen in the 50 mT/min nickel silicide traces in Figure 2.24a and the 20 mT/min aluminium trace in Figure 2.24c. This rules out eddy current heating, which depends only on the *rate* of change of magnetic field. We hence conclude that the most probable cause of the hysteresis is heating by *adiabatic demagnetization*.

Heating and cooling by adiabatic demagnetization can be understood by considering the total entropy in a magnetic system. There are two main contributions: the magnetic entropy of unaligned magnetic moments and the thermal entropy of a finite temperature. Imagine we begin with a collection of magnetic moments at 100mK and no applied magnetic field. We now very slowly begin applying a magnetic field, causing the magnet moments to align and thereby lower the total entropy. Assuming good coupling to the thermal bath, by the second law of thermodynamics $dS = \frac{dQ}{T}$ this change in entropy dS can be compensated by a heat flow dQ to the bath such that the temperature T is not altered. Contrast this with a situation in which we ramp up the magnetic field faster than heat can be transferred to the bath (i.e. adiabatically). With no heat flow dQ, the second law of thermodynamics tells us we cannot have any change in entropy dS. The decrease in magnetic entropy is thus compensated by an increase in thermal entropy - the temperature has increased. The same argument applies in reverse and can be used to cool samples.

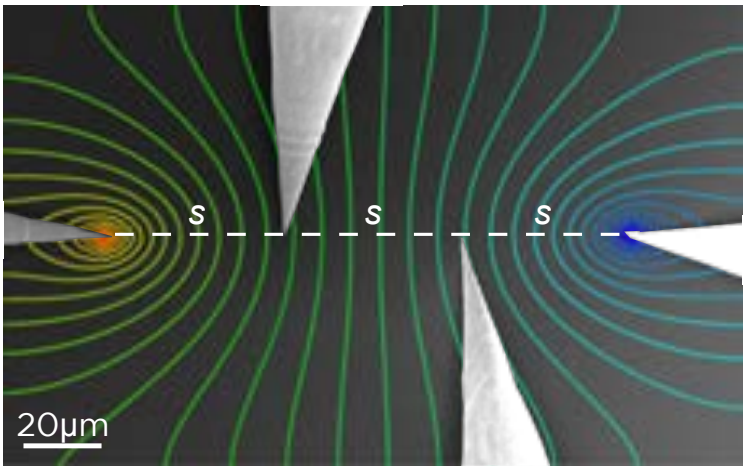
Since we are in the weak localization regime, cooling the sample would raise the resistance while heating would reduce it. In Figure 2.24 we consistently see only a heating effect - sweeps towards zero field are not changing with the sweep rate, while sweeps away from zero field exhibit a dip in the magnetoresistance (the clearest demonstration of this is in the aluminium traces in Fig. 2.24c). This is most likely due to the cryostat already being at base temperature and hence at the limit of how much heat it can remove. A small amount of sample heating is hence possible, but further sample cooling is not.

2.5 Conclusions

We began this chapter by highlighting the need for a new Ohmic contact metallization to improve on the aluminium based scheme developed by Rueß 8 years ago. After identifying nickel silicide as a promising candidate, we have developed a complete processing recipe suitable for STM-patterned silicon dopant device architectures. The largest portion of the thermal budget in this new process at present is a furnace anneal to 300°C for 30 minutes. While dopant diffusion is not expected to be a factor under these conditions, with the guidance of appropriate characterization techniques it should be possible in future work to further reduce this time and temperature if desired.

Having developed this process, we then performed a detailed comparative study of the low-temperature magneto-transport properties of an aluminium and a nickel silicide contacted Si:P δ-layers. We were able to show that a nickel silicide contact is comparable to aluminium, with the added advantage that nickel silicide does not transition to a superconducting state at milliKelvin temperatures. This eliminates a related contact resistance artifact, which we were able to study in detail using the aluminium control sample. In addition we could show that the silicide contacts did not contribute to rate dependent magnetic field hysteresis. Instead we were able to link this hysteresis to adiabatic demagnetization of magnetic material within either the cryostat or the sample carrier packages.

A journal article summarising the results of this chapter has been published in Nanoscale Research Letters[17]. The contacting process we have developed in this chapter has also been employed to fabricate δ-doped samples for low-frequency noise measurements, the results of which are published in Physical Review B[77]. We believe the nickel silicide process developed in this chapter will remain relevant not only for future sensitive characterization experiments but also emerging multilayer device architectures[78] where a highly controllable contacting depth may be helpful. It is also a good starting point for work on germanide contacts for atomic-scale dopant devices in germanium[79].



Four point probe resistivity measurements of δ-doped silicon

Index of key results and discussions

For introductory material covering four-point probe measurements, refer to section 3.1 on page 51. For specific information about the Omicron Nanoprobe system, refer to section 3.1.3.

For discussion about applying the four-point probe technique to a bulk-doped silicon substrate, refer to section 3.2 on page 61. Specifically, discussion of I-V characteristics can be found in section 3.2.2, probe-spacing dependent four-terminal measurements in section 3.2.3 and temperature dependent measurements in section 3.2.4. The important role of surface Fermi-level pinning is discussed in section 3.2.3.2.

Measurements of electrically active δ-layers begin in section 3.3 on page 83, covering the fabrication technique as well as I-V and probe spacing dependent measurements.

Section 3.4 on page 87 is concerned with thoroughly proving that four-probe measurements are unaffected by parallel conduction through the substrate. Evidence is drawn from two-terminal measurements in section 3.4.1 and temperature dependence measurements in section 3.4.3. We exclude the possibility of the observed conduction being due to the encapsulation layer on page 89 and metallic surface states on page 90. Calculations of how multi-layered conduction would appear in our measurements if present are shown in section 3.4.4

A model to explain the apparent electrical isolation of the δ-layer and the substrate is offered in section 3.5, based on spreading resistance considerations.

For a journal article summarising the results of this chapter, see reference[80] - Polley *et al*, Applied Physics Letters **101** 262105 (2012).

3.1 Four-point probe measurements

The four-point probe characterization technique forms the basis of this and subsequent chapters. In this section we review the concept of four-probe measurements, and their application for determining material resistivities. We also review the technical details of the Omicron Nanoprobe system used to perform the measurements in this thesis.

Suppose that you were given an unmarked resistor, how would you determine its resistance? The realistic (if trivial) answer is put the probes of your digital multimeter across it and look at the reading (Figure 3.1a). In a very direct application of Ohm's law, the meter is applying a known voltage across the terminals and measuring how much current flows ($V = IR$). In this chapter we will be taking the inverse approach, where a known current is applied and the resulting potential difference is measured.

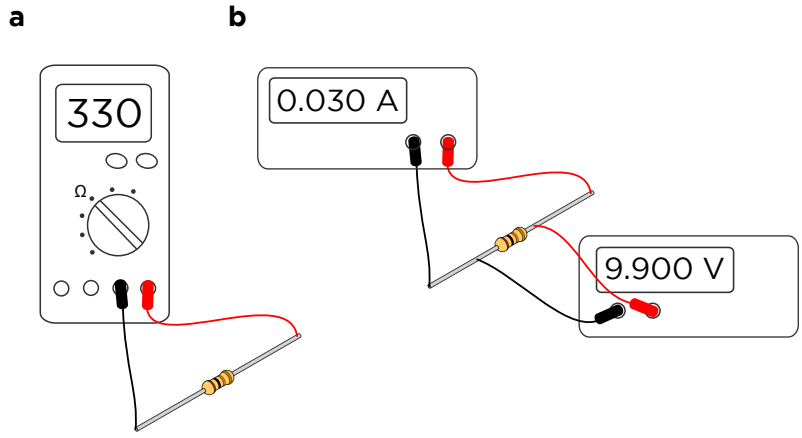


Figure 3.1: **How to measure a resistor** The conventional, two-terminal method of measuring resistance (a) is adequate for a wide variety of circumstances. In cases where the properties of the current sourcing probes become important to the measurement accuracy, a four-terminal technique (b) is required.

The problem with such a measurement technique is that we are measuring the potential difference across not just our unknown resistor but the *entire measurement system* (multimeter internals, probe leads, resistor legs ...). In many cases this error is of little consequence - we will overestimate by a few mΩ, which is typically less than the manufacturing tolerance for commercially available resistors. But cases exist in which this extra resistance is comparable to what we are trying to measure. In such cases the solution is to 'remotely' source the current, but 'locally' measure the potential (Figure 3.1b). This is called a **four terminal resistance measurement**. In doing this you have satisfied

both of the criteria for an accurate resistance measurement: all of the current is passing through the resistance of interest, and the voltage you are measuring arises solely from the resistance of interest.

We lose this certainty about the current once we go beyond discrete resistors with well-defined dimensions and try to measure the resistivity of some sheet or volume of material. In this context we usually refer to the four terminal configuration as **four probe**. In contrast to our 1-dimensional resistor, current now spreads out everywhere in the sample, and the geometry of the system must be considered to relate the potential difference we measure to the fraction of the current which caused it (Figure 3.2). This uncertainty about how current is distributed is one of the major challenges in performing 4-probe measurements.

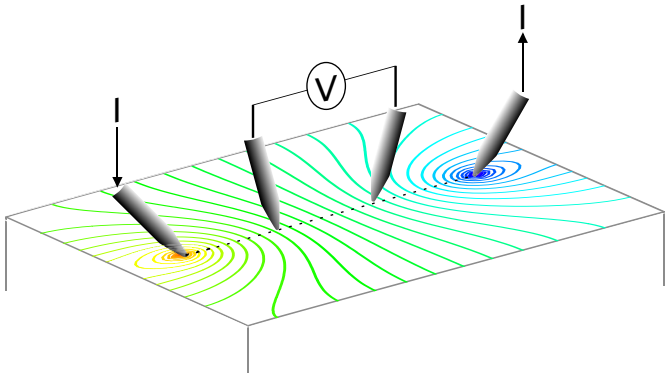


Figure 3.2: **Four probe measurements in 2 or 3 dimensions** A simulated contour map of the potential at the surface of a 3 dimensional sample passing a current between the two outer probes. The inner probes measure a potential difference on the surface, but the geometry of the sample must be considered to deduce the fraction of the current which passes between the measurement probes.

3.1.1 Extracting resistivity

In Figure 3.2 we see that the two outer current probes ('sourcing' and 'draining' current) have created a varying potential across the entire sample surface. The two measurement probes can be placed completely at random and will measure a potential difference, which can be combined with the source/drain current to generate a resistance, $R_{4T} = V_{4T}/I_{SD}$. In order to map this configuration-dependent *resistance* into a configuration-independent material *resistivity*, we must be able to determine the current flow within the sample. For this reason certain symmetrical probe placements are preferred in order to simplify the mathematics involved. By far the most common of these configurations, and the one we will use almost exclusively in the following two chapters, is the collinear arrangement depicted in Figure 3.2 in a source-measure-measure-drain configuration. Relating the four-terminal resistance to the material resistivity can then be accomplished

with the Laplace equation, capitalizing on symmetries in the configuration. The derivation is lengthy and reserved for Appendix A, but we state the key results here. For a 3 dimensional, homogeneous, semi-infinite material (meaning infinite in lateral extent and depth) we obtain:

$$\mathrm{R_{4T}} = \frac{\rho}{2\pi s} \qquad \text{(3D)} \tag{3.1}$$

where s is the probe spacing, ρ the bulk resistivity (i.e. Ωcm) and R_{4T} the four terminal resistance, defined as the potential difference across the measure probes divided by the current sourced through the source/drain probes. In cases where the substrate depth is much less than the probe separation we can consider the substrate to be two dimensional, and a similar mathematical treatment gives a new mapping:

$$\mathrm{R_{4T}} = \frac{\rho_S \ln(2)}{\pi} \qquad \text{(2D)} \tag{3.2}$$

with ρ_s the sheet resistivity (i.e. $\Omega/\square$). We will discuss these equations and modifications to them in subsequent sections, but for now we highlight a significant difference in the functional forms of Equations 3.1 and 3.2. In a 3D system the four-terminal resistance scales inversely with the probe separation, while in a 2D system it is independent of probe separation. The consequence is that a set of measurements performed as a function of s can easily distinguish transport through a bulk substrate (R$\propto \frac{1}{s}$) or a 2 dimensional surface layer (R=constant)[81;82]. This result is of major significance to this chapter, and will be used extensively in later sections to distinguish between a 2D dopant layer and the 3D substrate it is formed on.

3.1.1.1 Alternative measurement configurations

In the preceding discussions we assumed the most conventional collinear four-probe measurement arrangement, where the outer two probes source and drain the measurement current and the inner two probes measure the surface potential. Four different measurement functions (source current, measure high, measure low, drain current) are assigned to the four different probes, thereby making 4! = 24 possible configurations, which we show in Figure 3.3. The use of 'alternative' configurations has some useful applications, so in preparation for subsequent discussion we will briefly discuss these configurations here.

We begin by noting that no new information is obtained if we simply swap the two voltage measurement probes. Assuming there is no offset in the instrument, all that changes is the polarity of the measured voltage. We therefore do not forfeit any information by eliminating any permutations that swap the voltage measurement probes M_H and M_L, and this reduces our list to 12 permutations.

We may then further reduce this list by assuming we will sweep the source-drain current over both polarities - for example, from -10 $\rightarrow$ 10μA. This effectively swaps the

source and drain probes as we pass through 0. In many cases the sample conductivity can be expected to be the same in all spatial directions, in which case we should expect measurements to be symmetrical about I=0. This reduces the list to 6.

Finally, we may narrow it even further by assuming homogeneous conductivity (i.e. if the sample were rotated underneath the probes, the measured conductivity would not change). This makes pairs such as (S-D-M_H-M_L , M_L-M_H-D-S) redundant. The three configurations that remain, denoted 1, 2 and 3 are not reducible further. As will be shown in later sections, performing measurements in multiple configurations can provide information about the substrate geometry and the accuracy of probe placement without the inconvenience of physically repositioning the probes.

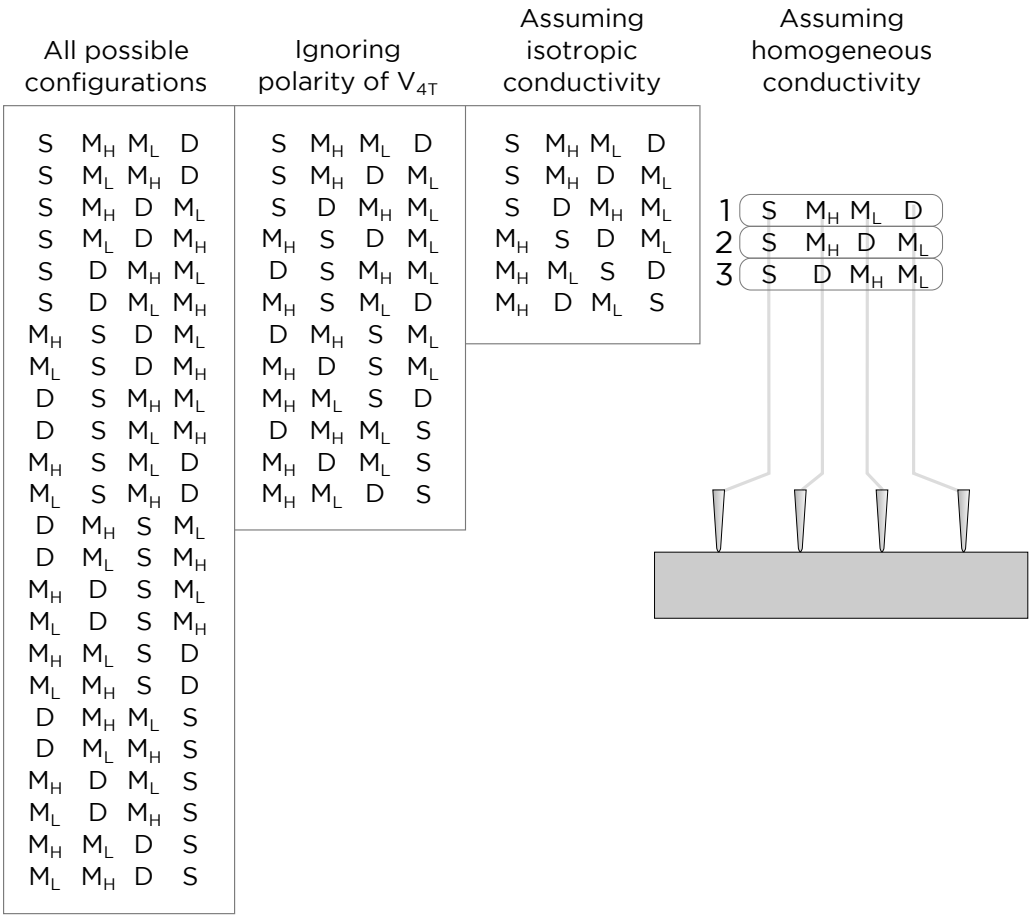


Figure 3.3: **Unique permutations of a 4 terminal measurement configuration** A listing of measurement permutations, where S is the current source, D the current drain and M_H and M_L the high- and low-side of a potential measurement. The number of unique permutations can be reduced to only three by symmetry considerations.

3.1.1.2 Definitions and nomenclature

Before proceeding, we should take a moment to clarify the nomenclature and a few of the concepts so far:

- *Probe spacing* will always refer to the equidistance between each probe in a collinear configuration. In any cases where we need to refer to some different kind of probe separation, this will be made explicit.
- *Four-terminal measurement* will henceforth be interchangeable with *four-probe measurement*, both meaning a four-terminal resistance measurement using repositionable probes.
- *Resistance* is the constant of proportionality between a voltage and a current. It does not necessarily have any direct physical meaning.
- *Resistivity* is a material parameter indicating what resistance will be obtained for a given amount of material. The units of resistivity depend on the geometry of the material.
- *Sheet resistance (ρ_S)* or equivalently *sheet resistivity* is the resistivity of a 2 dimensional material. It is stated in units of Ohms per square, with the interpretation that the resistance between opposing edges of any sized square of the material will be ρ_S
- *Bulk resistivity (ρ)* is the resistivity of a 3 dimensional material. It is typically stated in units of Ohm-centimeters, with the interpretation that the resistance between opposing faces of a 1 cm^3 cube of the material will be ρ

3.1.2 Sources of error and other considerations

Equations 3.2 and 3.1 correspond to a theoretical, ideal four point probe measurement, but real substrates are not semi-infinite and real probes are not infinitely small. Such perturbations can be incorporated through the use of correction factors $F_1 ... F_N$. These can be calculated by a variety of mathematical techniques, most commonly the Laplace equation[83], method of images[84] or conformal mapping[85]. Here we will simply state the results of such calculations.

For the measurements presented in this thesis, the most important correction factor is that for finite sample depth. Equation 3.1 applies in cases where the sample depth t is much greater than the probe spacing s, while 3.2 applies if $t \ll s$. In intermediate cases, a depth correction factor F_1 must be applied:

$$R_{4T} = \frac{\rho}{2\pi s F_1} \tag{3.3}$$

where

$$F_1 = \frac{t/s}{2\ln\left(\frac{\sinh(t/s)}{\sinh(t/2s)}\right)}$$

F_1 smoothly links equations 3.1 and 3.2, tending to 1 at the 3D limit ($t \gg s$) and $ln(2)/2s$ at the 2D limit ($t \ll s$). This form of F_1 applies for samples with an insulating bottom surface, which is the only case we will encounter in this thesis. Qualitatively, F_1 has the effect of increasing the four terminal resistance at large probe spacings, reflecting the effect of current 'hitting the bottom' of the sample and thereby being constricted.

3.1.2.1 Finite planar extent of substrate

A similar correction factor exists to compensate for the finite lateral extent of the sample (current 'hits the walls'), and still another for the case where the probes are not positioned at the centre of the sample (the 'walls' are not symmetrically located with respect to the probes). These are outlined in detail in Schroder[86]. In this thesis we use probe spacings which are small with respect to the sample dimensions (typically ≈ 100 μm compared to a sample width of 2.5 mm), so these corrections amount to ≈2% at most. To simplify the analysis we have therefore not applied them, but have taken care to keep the probes as centered as possible within the sample when taking measurements.

3.1.2.2 Finite probe size

Equations 3.2 and 3.1 both assume infinitesimal point contact probes, which is unrealistic. Incorporating a finite probe size introduces two distinct considerations. Firstly it offsets (by the contact radius) the location at which current enters and exits the sample. This is critical for the evaluation of two-terminal resistance, which we will treat in more detail in subsequent sections, but also modifies Equations 3.2 and 3.1 to:[87]

$$\mathrm{R_{4T}} = \frac{\rho}{\pi}\left(\frac{1}{s+r} - \frac{1}{2s-r}\right) \qquad \text{(3D)} \tag{3.4}$$

$$\mathrm{R_{4T}} = \frac{\rho_S}{\pi}\ln\left(\frac{2s-r}{s+r}\right) \qquad \text{(2D)} \tag{3.5}$$

Where the probe contact is treated as a circle with radius r. Such corrections are only relevant at very small probe spacings; typically in this thesis we go to a minimum of 50 μm with probe radii of ≤500 nm, in which case the correction again amounts to ≈2% at most.

The second consequence of a finite probe size is that the two measurement probes represent regions of very high conductivity, effectively shorting the area of sample beneath them. This is difficult to treat analytically since it breaks the symmetry of the problem, however it is again only an issue at very small probe spacings.

3.1.2.3 Incorrect probe placement (not equidistant or not collinear)

Continuing to acknowledge reality, it is unlikely that the probes will be positioned perfectly collinear and equidistant (Figure 3.4a). Off-axis errors are difficult to treat analytically as they eliminate symmetry, but they can be mapped onto equivalent inline errors if the form of the surface potential is known by following an equipotential contour (shown in Figure 3.4b).

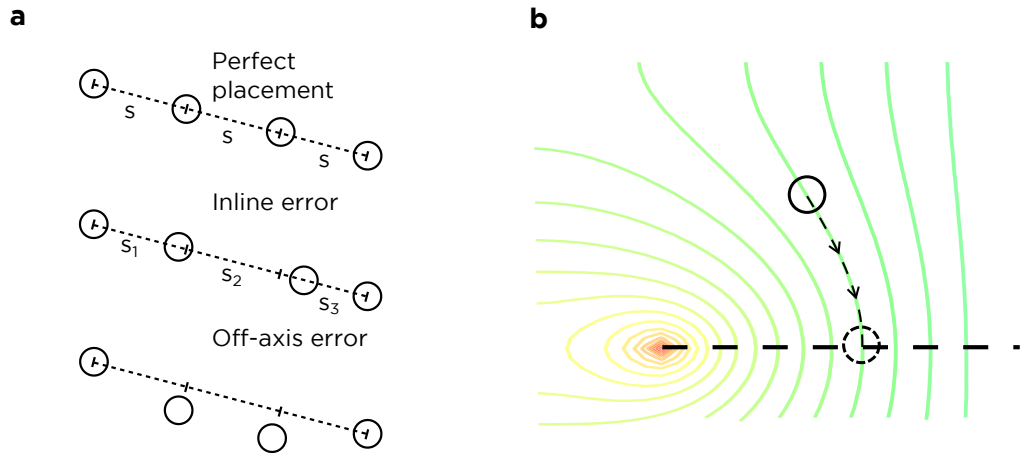


Figure 3.4: **Classification of positioning errors for a collinear four-probe measurement** All probe placement errors may be classified as inline or off-axis (a), though in principle the two are interchangeable by moving a probe along an equipotential contour (b).

Inline errors can be treated by using more general forms of Equations 3.2 and 3.1 where we do not assume equidistant spacings (see Appendix A). With reference to Figure 3.4a:

$$\mathrm{R_{4T}} = \frac{\rho}{2\pi}\left(\frac{1}{s_1} + \frac{1}{s_3} - \frac{1}{s_1+s_2} - \frac{1}{s_2+s_3}\right) \qquad \text{(3D)} \tag{3.6}$$

$$\mathrm{R_{4T}} = \frac{\rho_S}{\pi}\left(\ln\left(\frac{s_1+s_2}{s_1}\right) + \ln\left(\frac{s_2+s_3}{s_3}\right)\right) \qquad \text{(2D)} \tag{3.7}$$

By the method of partial derivatives, uncertainty in the inter-probe spacings Δs_n can be propagated through to the uncertainty in measured resistance:

$$\Delta R_{4T} = \pm\sqrt{\left(\frac{\partial R_{4T}}{\partial s_1}\right)^2(\Delta s_1)^2 + \left(\frac{\partial R_{4T}}{\partial s_2}\right)^2(\Delta s_2)^2 + \left(\frac{\partial R_{4T}}{\partial s_3}\right)^2(\Delta s_3)^2} \tag{3.8}$$

A script to perform this calculation is contained in Appendix B. For a reasonable 'worst case' estimate of a probe spacing of 100 μm with spacing uncertainty of ± 5 μm (5% relative error), we obtain an uncertainty in resistance of $\approx$5.3% if the sample is 3D and $\approx$4.0% if it is 2D. Over a wide range of values the error in resistance is approximately equal to the relative error in probe separation.

The Nanoprobe system has the important advantage of an *in situ* electron microscope, making it possible to verify the probe positions for each measurement. Placement accuracy within 2% becomes straightforward, and if desired the remaining error could be further reduced by measuring the s_n from the SEM image and applying Equations 3.6 and 3.7 instead of 3.1 and 3.2.

Alternatively, if four-probe measurements are taken in more than one measurement configuration (Figure 3.3) and the transport channel is known to be two-dimensional, positioning errors can be canceled with the dual-configuration expression of Rymaszewski[85], essentially a special case of the van der Pauw problem. As an example, resistance measurements obtained from configurations 1 and 2 on a 2D sample satisfy:

$$\exp\left(\frac{-\pi R_{4T,1}}{\rho_s}\right) + \exp\left(\frac{-\pi R_{4T,2}}{\rho_s}\right) = 1 \tag{3.9}$$

The value of ρ_s obtained from solving this equation is unaffected by probe positioning errors. This technique is only applicable to 2D samples, which is clear from the fact that it is derived from conformal mapping of a 2D potential but has also been explicitly shown experimentally[88]. We will spend much of this thesis measuring samples for which it is not obvious *a priori* whether conduction is purely 2D; as such we have avoided using the dual-configuration correction.

3.1.2.4 Measurement equipment

The three required items of measurement equipment for a four-probe measurement are a precision power supply to provide a stable measurement current, an ammeter to accurately measure the total current entering the sample and a voltmeter to measure the potential across the two measurement probes. It is important that the current can be swept over a range of values. A single measurement is likely to be influenced by offsets in the ammeter and voltmeter, while a linear fit to a range of data will eliminate offsets.

The voltmeter must have a sufficiently high input impedance that it does not represent a shunt path. A voltmeter which draws current has two consequences: the region being probed is seeing less current than we assume, and the measurement probes now pick up additional potential drops from the current across their contact resistance. What constitutes a 'sufficiently high' input impedance depends on the sample being measured; ideally the input impedance should be at least an order of magnitude higher than the four-terminal resistance. Throughout this thesis we have employed the 6514 electrometer from Keithley which has an input impedance of $>$200 TΩ, far in excess of anything we measure.

Another consideration is the common mode rejection ratio (CMRR) of the voltmeter. In a typical four-probe configuration the source has some applied bias V while the drain is held at ground. The voltage probes are hence measuring a small differential voltage on top of a large background of $V/2$. The ability of the voltmeter to perfectly cancel

this common background is crucial to an accurate voltage measurement. Any unrejected common mode signal will be amplified and appear as an offset in the instrument output. The 6514 electrometer has a CMRR>120 dB at DC, meaning the common mode voltage is attenuated by 1×10^6. To understand the impact of these numbers, we can look at some typical 'worst-case' measurement values from an undoped substrate. From an applied source-drain voltage of ±1 V we might measure a four-terminal voltage of ±1 mV. The 1 V would result in a common mode voltage of 0.5 V, which after 120 dB reduction results in a four-terminal voltage error of 500 nV, a relative error of only 0.05%.

It is worth noting that CMRR is degraded approximately linearly with the logarithm of frequency. Even with a nominally DC measurement, if the probes are mechanically vibrating such that the contact resistance is changing rapidly, the common mode voltage would become AC. Using numbers from the previous paragraph, lowering the CMRR to 80 dB would increase the voltage reading error to 5%. The frequency behaviour of the 6514 is not published, but for an estimate one can look at high-end instrumentation amplifiers such as the INA128[89] or AD620[90]. For these parts the CMRR degrades by 40 dB only for frequencies higher than $\approx$10 kHz, well above typical mechanical noise frequencies. We thus do not believe this effect is significant in our measurements.

For a meaningful four-probe measurement the conduction through the sample must be Ohmic (i.e. current proportional to voltage), but there is no such requirement for the probe contacts. In essence, provided that the ammeter can tell you *how much* current is entering the sample it is not directly relevant *how* it enters.

3.1.3 The Omicron Nanoprobe

The four-probe work contained in this thesis is performed with a UHV Nanoprobe system from Omicron Nanotechnology GmbH. This system comprises two coupled UHV chambers (P$\approx5\times10^{-11}$ mBar), one dedicated to sample preparation and the other to four-probe measurements. The measurement chamber is equipped with 4 independent STM probes (Figure 3.5a), the defining feature of the system. Three of the probes are capable of resolving atomic terraces on silicon, while the fourth has been modified for higher resolution imaging (Figure 3.5c). With this probe, resolution of Si(100) 2×1 dimer rows is possible. At any given time only one probe can be used to record STM images; the significance of the other probes being STM is for automatic, non-destructive sample approaches and fine positioning control. Vibration isolation is achieved by a Viton stack at the stage and pneumatic air-legs to raise the entire system off the ground.

For the probes we use electrochemically etched polycrystalline tungsten wire. These can be annealed *in situ* by an electron-beam bombardment system to ensure clean, oxide-free tips for electrical measurements. To enable versatile electrical measurements, each probe is wired to an *ex situ* BNC connector. For the contents of this thesis, measurements are performed with a 236 source-measure unit and 6514 electrometer, both from Keithley. A switching matrix allows rapid changes between arbitrary measurement configurations.

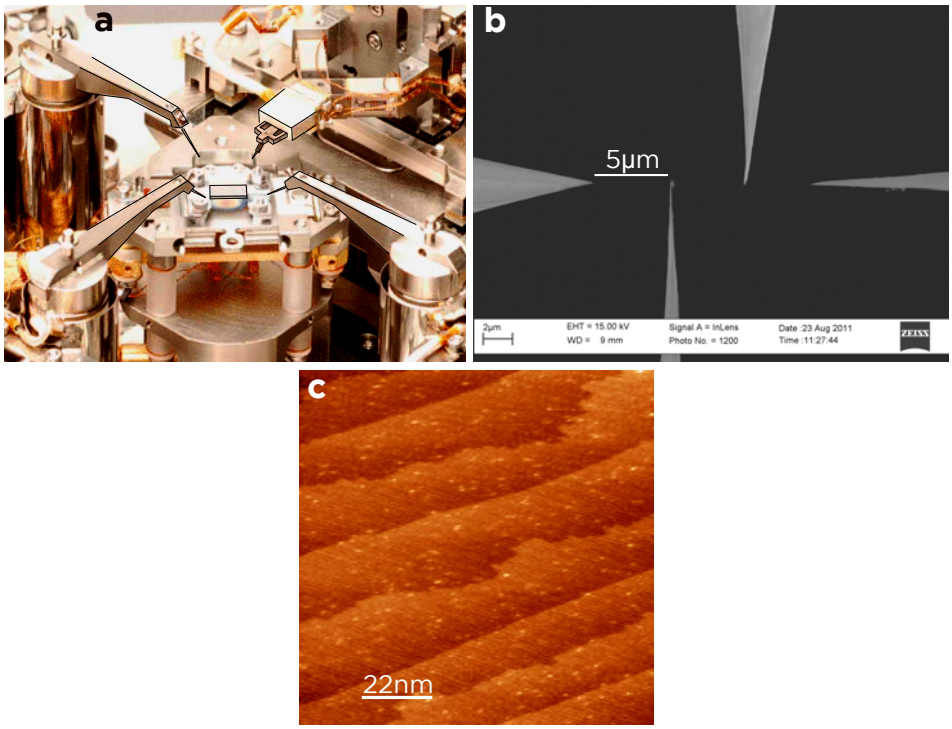


Figure 3.5: **The Nanoprobe system from Omicron** The key feature of the Nanoprobe system is a sample stage with 4 independent STM probes (a), under the observation of a high-resolution *in situ* electron microscope (b). In STM imaging mode, resolution of atomic terraces on the Si(100) 2×1 surface is straightforward (c).

Also contained in the measurement chamber is a 'Gemini' scanning electron microscope, with an in-lens secondary electron detector and <5 nm resolution. This is mounted directly above the sample stage, and is critical for correct positioning of the STM probes (Figure 3.5b).

The sample holders accept rectangular samples (2.5 mm × 10 mm) which are suspended above a metallic baseplate, clamped at each end (Figure 3.6). Insulating washers are in place on one of the clamps, such that only one side of the sample has an electrical connection to the baseplate. An external BNC connection to the baseplate is provided along with the four probes, allowing the sample to be grounded or left floating. The sample stage incorporates a solid state heater and liquid helium flow cryostat to enable control of the sample temperature from 30 K to 500 K. A Pt100 resistor in the sample stage provides accurate temperature readout.

The sample preparation chamber contains a sample-heating stage (both electron-beam and direct-current), with an *ex situ* infrared pyrometer for monitoring the sample temperature. This chamber also contains dosers for phosphine gas and atomic hydrogen, together with a high-resistivity silicon sublimation cell for epitaxial silicon growth (at ≈ 3 Å/min).

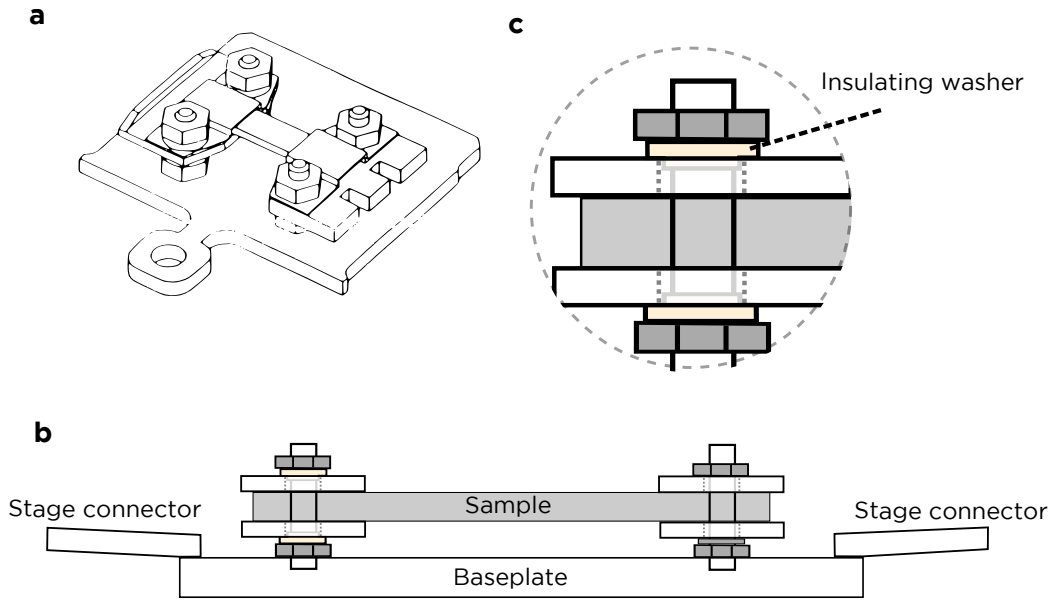


Figure 3.6: **The Nanoprobe sample holder design** The Nanoprobe sample holder (a) clamps rectangular samples above a metallic baseplate, which is electrically connected to the sample stage (b). Insulating washers on one end of the sample holder (c) ensure that only one side of the sample is connected to the baseplate (avoiding a parallel conduction path).

3.2 Characterizing the substrate

Having introduced the four-point probe measurement system, in this section we discuss intial measurements of lightly doped silicon substrates. The eventual goal of this chapter is to measure the resistivity of a δ-doping profile in silicon, but if we hope to understand such a measurement it is crucial that both the undoped substrate and this relatively new measurement technique be well understood first. In this section we will explain the measurement methodology in detail. Measurement results will begin with an investigation of single probe I-V characteristics, which contain information about the physics underlying the probe-sample contacts. We will then show four probe measurements of a variety of silicon substrates of known dimensions and resistivities, validating the use of Equations 3.1 and 3.2. We will discuss the role of Fermi level pinning at the silicon surface for single- and four-probe measurements, before finally discussing low-temperature measurements of a lightly doped substrate.

3.2.1 Experimental method

Sample preparation

For the experiments in this thesis we use samples cleaved from commercially available Si(100) wafers, with nominal miscut angles of ± 0.1 °. Prior to entering the UHV system, samples are repeatedly chemically cleaned in a sequence of:

1. Piranha etch (H_2SO_4:H_2O_2) to remove organic contaminants
2. Dilute hydrofluoric acid to remove surface oxide
3. RCA-2 (H_2O:HCl:H_2O_2) to remove metallic contaminants

Upon entry into UHV, samples are outgassed in a two stage process. First the entire sample holder is held at ≈400 °C for ≥6 hours by electron-beam heating. Following this, direct-current heating is used to hold only the silicon at ≈500 °C for ≥6 hours. To obtain clean reconstructed silicon surfaces, the sample is then rapid thermal annealed by direct current heating to 1100 °C (after the method of Swartzentruber[22]). This method reliably produces contamination free, low defect-density surfaces as can be verified by STM imaging.

Tip preparation

The STM probes used throughout this thesis are created by electrochemically etching polycrystalline tungsten wire (further discussion of the procedure is contained in chapter 5). Once a probe has been etched it is rinsed in a ≈70 °C deionized water bath to remove residual etchant solution. There are stringent geometrical requirements for both the nano-scale tip and micro-scale taper of the probes, so etched tips are culled by observation with an electron microscope. Once a sufficient number of suitable probes are obtained, they are baked in a high vacuum loadlock at 150 °C for >12 hours (primarily to desorb water). Once transferred into UHV they are annealed *in situ* by electron bombardment to desorb any tungsten oxides that may have formed and ensure a clean contacting interface.

Tip approach

Once probes and a sample are prepared for a measurement, the probes must be approached nondestructively to the sample surface. We perform this by first coarse approaching to within $\approx 500\ \mu$m by eye, then covering the remaining distance automatically with STM feedback control. Once the tips are within tunneling distance, the feedback loop is disengaged and the probes manually driven into physical contact with the sample to establish a satisfactory electrical contact (in the following section we will elucidate what constitutes a 'satisfactory' contact). The system is well isolated against vibration, so unless the sample is being cooled and thermal contraction is an issue, tip-sample contacts are highly stable over the 1-2 minutes of a typical measurement.

3.2.2 Tip-to-sample I-V characteristics

The simplest type of measurement we can perform is a current-voltage sweep between a single probe and a grounded substrate. This is an important technique for confirming that all probes have made good electrical contact with the sample before beginning a 4-terminal measurement, but also contains basic information about the sample being measured. While it is difficult to extract reliable quantitative information from such measurements, we will see that they contain useful qualitative information about the sample and the nature of current injection. This information will prove useful when interpreting 4-probe measurements.

3.2.2.1 Measurement details

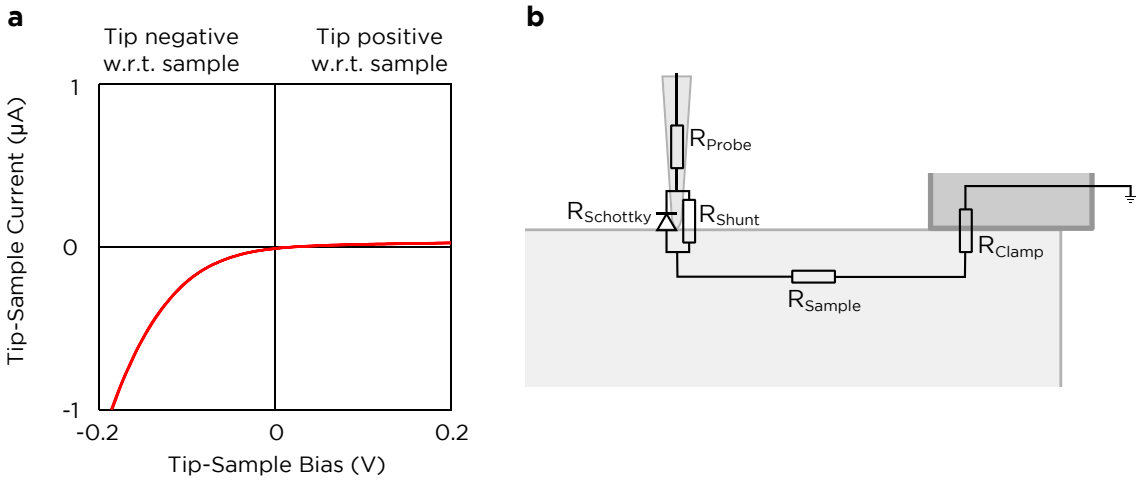


Figure 3.7: **Single probe I-V measurements** In a single probe measurement the sample is grounded through the clamp and a bias is applied to a single probe in contact with the sample. Rectifying current-voltage behaviour is observed (a), as expected for a metal-semiconductor contact. Several different elements contribute to this measurement, schematically depicted in (b).

In a single-probe I-V measurement (Figure 3.7) one end of the sample is grounded and a ramped DC bias is applied to one of the probes while recording the current flow. All other probes are left electrically floating. Figure 3.7a demonstrates a typical measurement obtained from a semiconducting substrate. The main drawback of such a measurement (and the reason why four-probe measurements are important) is that it contains *too much* information; there are many different components contributing to the measurement and it is difficult to separate out parameters of interest. The schematic in Figure 3.7b illustrates the different components contributing to the measurement. We will briefly discuss each of these components to illustrate which of them are dominating the I-V characteristics.

R_{Probe}: The probe itself has some finite resistance R_{Probe}, having tapered to essentially a metallic nanowire at the point of contact. If we approximate our probe as a metallic truncated cone, we have:

$$R_{Probe} = \frac{\rho l}{\pi a b}$$

where l is the cone length, a & b the radii of the cone ends and ρ the resistivity of the probe material, in this case 5×10^{-6} Ωcm tungsten[91]. In Figure 3.8 we show representative SEM images of tungsten probes used in this thesis. While there is considerable variation in probe shapes, a coarse estimate of the probe dimensions as a truncated cone would be a length of 100μm, with end radii of 100 nm and 15 μm. These values yield a probe resistance of $\approx$ 1 ohm, which as we will shortly see is not a significant contribution by several orders of magnitude.

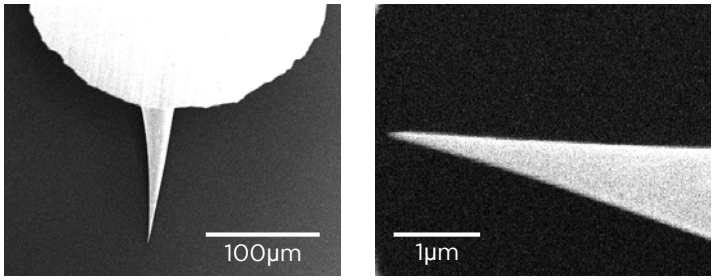


Figure 3.8: **High-resolution SEM images of the STM probes** High aspect-ratio, electrochemically etched tungsten probes are employed for measurements. The etched region of the probe tapers from a radius of $\approx$15 μm to less than 100 nm over a distance of $\approx$100μm. However due to the relatively high conductivity of metallic tungsten, the probe itself does not contribute appreciably to the measured resistance.

$R_{Schottky}$: At the point of contact with the sample there are two components in parallel: the metal-semiconductor Schottky barrier ($R_{Schottky}$) and Ohmic shunt paths (R_{Shunt}). We will group these together under the term 'interfacial resistance' (i.e. any resistance appearing only at the semiconductor surface). The *Schottky barrier* was discussed qualitatively in chapter 2. In the present context we are at room temperature and the substrate is lightly doped, so in terms of carrier transport we are firmly situated in the thermionic emission regime. The current through this element as a function of applied bias is then described by the Shockley diode equation:[92]:

$$I(V) = I_S(e^{\frac{\beta V}{n}} - 1) \tag{3.10}$$

where $\beta = \frac{q}{kT}$ is the inverse thermal voltage, n the 'ideality factor' and I_S the reverse bias saturation current, given by:

$$I_S = AA^{**}T^2 e^{-\beta\phi}$$

with A the contact area, A^{**} the modified Richardson constant, T the temperature and ϕ the Schottky barrier height. The ideality factor n is a phenomenological factor describing how well this model explains the measured data. If curve fitting requires deviation from $n = 1$ this indicates the occurrence of additional physical effects not captured by the model (such as leakage paths or tunneling currents). For typical values of the various parameters, I-V characteristics such as that shown in Figure 3.9 are obtained (and conventionally plotted as |ln(I)| vs V).

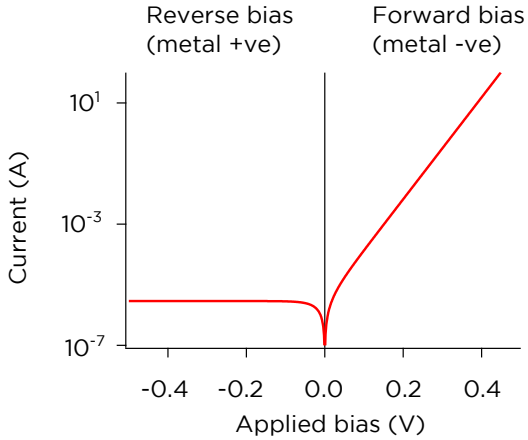


Figure 3.9: **Current-voltage behaviour for a metal-semiconductor contact in the thermionic emission regime** Equation 3.10 plotted using realistic values for a single-probe measurement of Si(100): A=3.1 μm^2, A^{**} = 112 A/cm^{2}K^2, T=300 K and ϕ=0.3 eV. Current is suppressed under reverse bias, and grows exponentially under forward bias.

In principle a large amount of information can be obtained from careful measurement and detailed analysis of Schottky I-Vs[93;94]. In the present context we are not concerned with performing quantitative analysis; it suffices to simply highlight the following key points:

- The current-voltage behaviour of the Schottky barrier is strongly rectifying, and furthermore this is the *only* element in Figure 3.7b which is nonlinear. This makes its contribution to the I-V characteristics easy to identify.
- The strength of rectification is directly related to the barrier height

R$_{\text{Shunt}}$: The second component to the interfacial resistance is the *shunt resistance* in parallel with the Schottky contact. This is always present to some extent in real measurements, and manifests as a non-saturating reverse-bias current. Physically it may originate from local Ohmic contact regions where the underlying silicon has undergone a beta-tin phase transformation under high pressure[95]. For the measurements in this thesis on lightly doped silicon samples, shunt resistances in the range of MΩ to GΩ are typical.

$\mathbf{R_{Sample}}$: Contrast this with the return path through the substrate, described by:[86]

$$R_{Substrate} = \frac{\rho}{4r} \tag{3.11}$$

where ρ is now the resistivity of the substrate and r the probe contact radius. With a 100 nm radius probe on a 7 Ωcm substrate, we obtain a resistance of ≈175 kΩ. The magnitude of this term is owed in large part to the very small contact radius, which constricts the current to a small volume until it manages to spread out into the full volume of the substrate. This effect is often termed a 'spreading resistance', but the definition is often nebulous. For subsequent discussions it will be helpful to briefly provide a rigid definition of this concept.

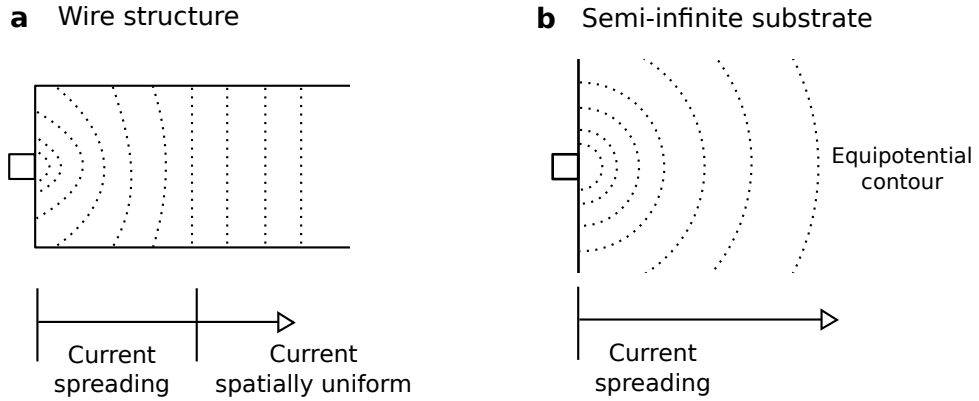


Figure 3.10: **Current spreading in samples of different geometry** In a structure with non-infinite dimensions such as a macroscopic wire, current injected from a small area contact requires some distance to 'spread out' (a). Beyond this distance the current becomes spatially uniform. In the case of a semi-infinite sample, current never ceases to 'spread out' (b).

To demonstrate the source of ambiguity in defining 'spreading resistance', in Figure 3.10 we schematically compare the current distribution from a point contact to a macroscopic wire structure (Fig3.10a) and a semi-infinite substrate (Fig3.10b). In a three (two) dimensional material, the resistance of a conductor scales inversely with the area (width) of the current path. Close to a point contact, current 'sees' a small region of material which represents a high resistance, while current that has spread out sees a much larger area and therefore a low resistance (compare for example the circumferences of equipotential lines in Fig3.10b). This phenomenon is often called *spreading resistance*, and is said to arise from *current crowding*. In a macroscopic wire structure (Figure 3.10a) carriers eventually encounter sidewalls, and the current distribution becomes spatially uniform. In such a context, it is possible to delineate between two regions of current flow and the resistance they represent: the *spreading* resistance and the *bulk* or *device* resistance. The length scales over which current spreads are often small compared to the entire conductor, and spreading resistance can quite reasonably be grouped with *contact resistance*. This

becomes problematic in a semi-infinite conductor (Figure 3.10b) where current *never stops spreading out*. In this case there can be no meaningful delineation between spreading resistance and bulk/device resistance, and it is no longer reasonable to include spreading resistance in contact resistance. Hence for the semi-infinite conductors we will study in this chapter, *spreading resistance* and *sample resistance* are completely equivalent. While potentially confusing, it is helpful to retain the term 'spreading resistance' since this reminds us that we must always consider the geometry of the current path.

R_{Clamp}: The final element in Figure 3.7 is the sample-to-clamp contact. While this is a second metal-semiconductor contact, the contact area of the clamp combined with the high pressure of the clamp contact result in a low resistance Ohmic contact. We can demonstrate this by the measurement shown in Figure 3.11a. By putting a probe on top of each clamp, we can measure the combined resistance of the substrate and both clamp contacts. Figure 3.7b shows the result of such a measurement, where we have obtained an Ohmic resistance of 9.1 kΩ.

The sample in this case has dimensions of 2.5 mm × 300 μm × ≈6 mm and a nominal resistivity of 75 Ωcm. We can therefore estimate the sample resistance in this configuration to be ≈6 kΩ (using R=ρL/A). The clamp contacts are hence contributing ≈ 1.5 kΩ each. This is a coarse estimate, but the important conclusion is that the sample-to-clamp contact in Figure 3.7 is Ohmic and two orders of magnitude less than the ≈175 kOhm estimated from probe spreading resistance considerations.

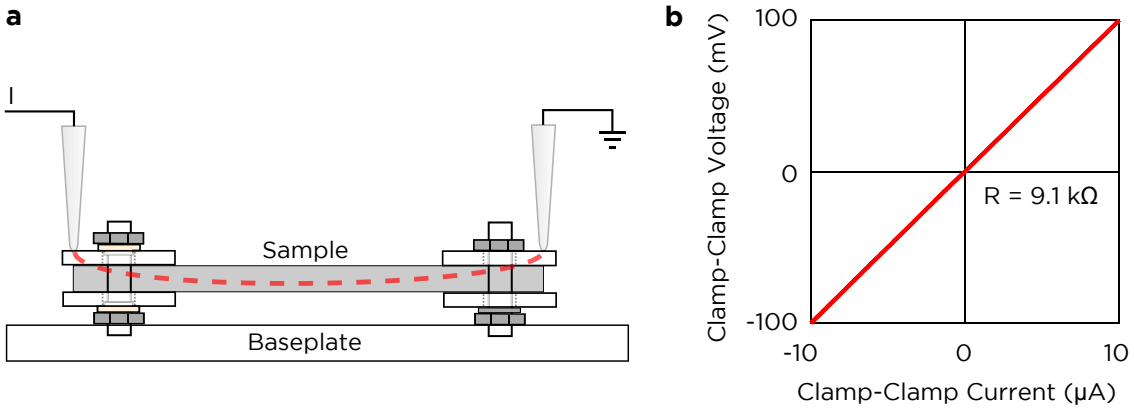


Figure 3.11: **Demonstrating Ohmic contact from the sample clamps** The nature of the clamp-sample contact can be investigated by placing a probe on each clamp (a). This yields a perfectly Ohmic current-voltage trace (b). The insulating washers on one of the clamps prevent a current path through the baseplate.

3.2.2.2 Definitions and nomenclature

The different components of this single-probe resistance measurement will recur throughout this chapter, so let us once again, summarize the new nomenclature:

- *Probe resistance* refers to the (Ohmic) resistance of the metallic probe itself, considered in isolation.
- *Interfacial resistance* is a blanket term collecting any resistance which originates solely at the probe-sample interface - we have discussed the Schottky resistance and shunt pathways as components of this term.
- The *Schottky resistance* arises from the potential barrier at the metal-semiconductor interface impeding current flow. It is typically non-Ohmic.
- A *shunt* is a general concept meaning a parallel current path, typically unintended. The *shunt resistance* discussed previously refers to the specific case of Ohmic current pathways at the probe-sample interface which bypass the Schottky resistance.
- *Spreading resistance, substrate resistance*. This is proportional to, but completely distinct from *resistivity*.
- *Contact resistance* is equivalent to *interfacial resistance* in this thesis, and neither encompass *spreading resistance*.

3.2.2.3 Single probe I-V measurement results on lightly doped Si(100)

Having discussed the individual components of a probe-sample contact, we are now in a position to understand I-V measurements on bulk doped Si(100) substrates (i.e. before δ-doping). In Figure 3.12a we show a schematic of the expected conductance ($\ln(\frac{dI}{dV})$) as a function of tip-sample bias V. Inset is an equivalent circuit diagram showing the relationship of the Schottky barrier, shunt resistance and series resistance. Plotting the conductance on a log scale highlights how different aspects of the contact dominate in particular bias regimes. When the metal-semiconductor junction is strongly forward biased it becomes essentially transparent, and the tip-sample current becomes limited by series resistance in the substrate and clamp (constant $\frac{dI}{dV}$). In intermediate biasing regimes the Schottky barrier dominates conduction ($\frac{dI}{dV} \propto \exp(V)$). At strong reverse biases, the Schottky contact becomes highly resistive, and conduction is dominated by the contact shunt resistance (constant $\frac{dI}{dV}$).

On this basis it is straightforward to interpret the experimental data in Figure 3.12b, which shows several separate single-probe measurements on a lightly doped p-type Si(100) substrate. With the Schottky barrier forward biased (tip-sample bias negative), all traces settle on essentially the same limiting conductance of $\approx 3 \times 10^{-6}$ ($\approx$300 kΩ). This

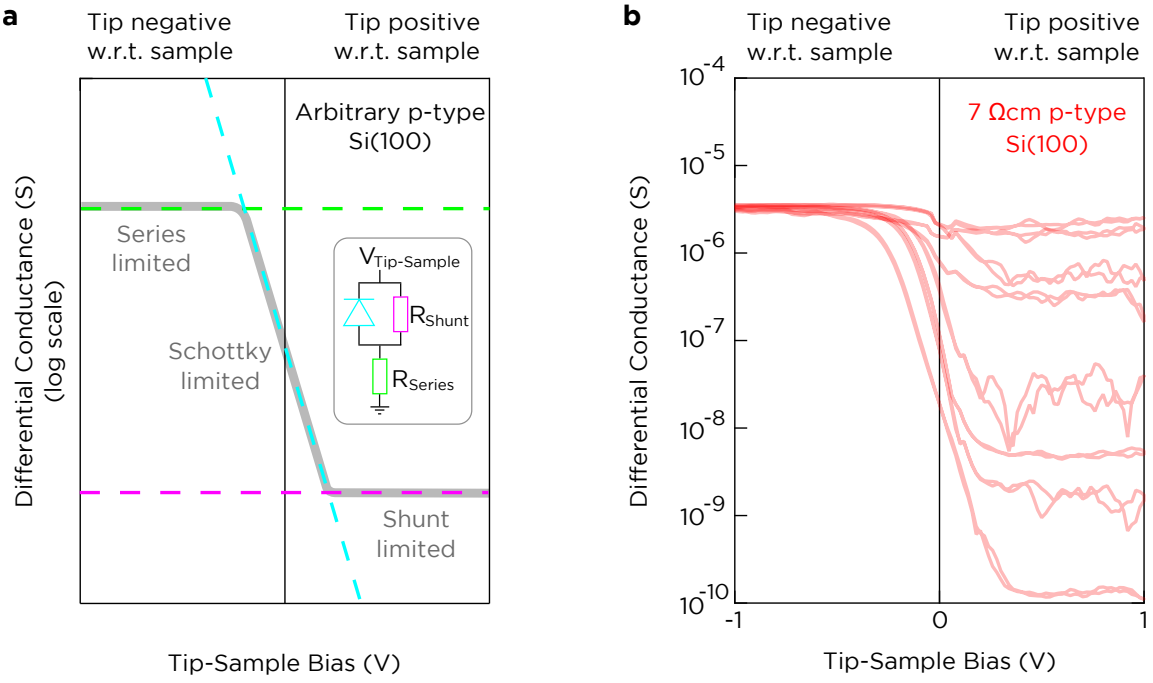


Figure 3.12: **Interpreting single probe current-voltage behaviour** (a) The bias dependent probe-sample differential conductance can be modeled in terms a three element equivalent circuit (shown in the inset). At high biases either the series or the shunt resistance provides a limiting conductance, with the Schottky element responsible for the transition between the two limits. Experimental data closely resembles this qualitative model (b).

value is comparable to our earlier, simplistic approximation of the substrate spreading resistance (Equation 3.11). In this approximation the resistance depends only on the contact area and the substrate resistivity; both of which are essentially unchanged with repeated contacting. When the tip is strongly forward biased the contact shunt resistance sets a lower limiting value, which varies by more than four orders of magnitude from contact to contact ($\approx$ 400 kΩ to $>$1 TΩ). The shunt resistance arises from complex interactions at the probe-silicon interface, and it is hence unsurprising that it should vary so much with repeated contacting.

In the preceding section we stated that the final stage of the tip approach procedure involved pushing the probes into the surface until a satisfactory electrical contact was established. We are now in a position to comment on what this is physically achieving. So far we have discussed measurements where we source current through a single probe and drain it through the large sample clamp. In contrast, a four-terminal measurement requires sourcing current from one probe and draining current through a second probe. As indicated by the equivalent circuit diagram in Figure 3.13 this means that at all times one of the probes will have a highly resistive reverse biased Schottky barrier. The important consequence of this is that the interfacial shunt resistances will always limit the

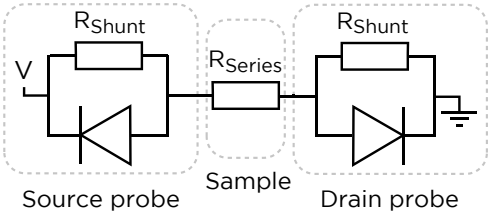


Figure 3.13: **The importance of shunt resistance** The equivalent circuit for a probe-to-probe measurement shows that under all bias conditions a Schottky element will be reverse biased and block all current flow. The parallel shunt resistance elements therefore dictate the total impedance of such a measurement.

current in a four-probe measurement. In order to make a reliable four-terminal measurement on these lightly doped substrates, it is therefore essential to establish low-resistance shunt paths at the contact. As demonstrated in Figure 3.14, this is what we are accomplishing by driving the probes into the sample. Here we have measured single probe I-V characteristics at 3 different stages of pushing the probe into the surface at various locations. The level of contact pressure cannot be directly measured, but we note that over this series of measurements the tungsten probes did not inelastically deform, and SEM observation of the sample surface after the measurements did not indicate any physical damage. As the contact pressure is increased the forward bias saturation conductance is increasing, corresponding to an increased level of shunting. The reverse bias saturation is also increasing, which is likely due to an increasing contact radius as the probes elastically deform.

3.2.3 Probe spacing dependent four-terminal measurements

In the subsequent sections we will study δ-doped silicon, and make extensive use of probe-spacing dependent four-probe measurements to determine whether the current flow is through the substrate or the δ-layer. To properly interpret such measurements it is vital that we first understand similar measurements of the substrate alone. In this section we will present and discuss 4-probe measurements of different silicon substrates at room temperature.

3.2.3.1 Experimental method

In section 3.1 we discussed the general methodology of 4 point probe measurements. To briefly summarize, we position the four probes on the sample surface collinearly and equidistant, as depicted in Figure 3.15a. A DC current is swept between the source and drain probes while the potential difference across the two measurement probes is recorded (Fig 3.15b). The gradient of a linear fit to this measurement yields the *four terminal resistance* R_{4T}. Depending on the thickness of the substrate relative to the probe separation, this resistance is related to the sample resistivity by either Equation 3.1 (thick

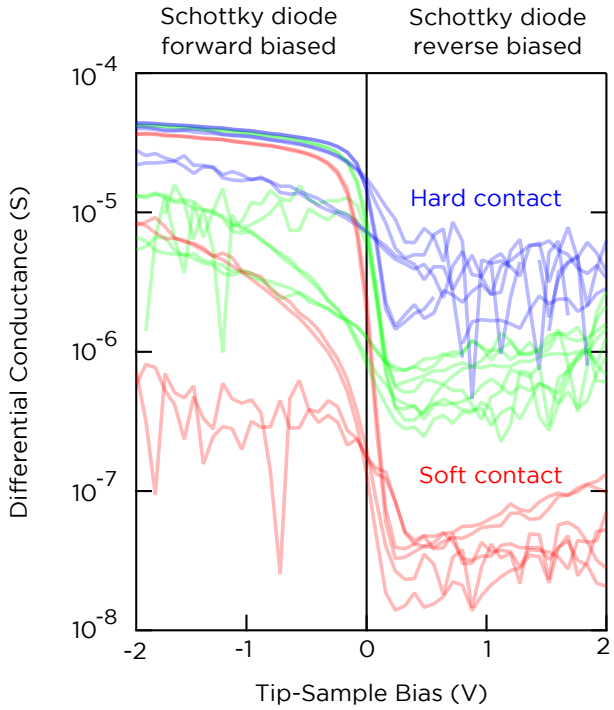


Figure 3.14: **The evolution of single probe I-V measurements with contact pressure.** Increasing the pressure of the probe-sample contact raises the reverse bias saturation conductance, which can be interpreted as an increased level of shunting.

substrate):

$$R_{4T} = \frac{\rho}{2\pi s} \qquad (3D)$$

or Equation 3.2 (thin substrate):

$$R_{4T} = \frac{\rho_S \ln(2)}{\pi} \qquad (2D)$$

In this section we will be performing four terminal resistance measurements as a function of the probe separation s for a variety of substrates. We limit the range of probe separations to (50 - 250) μm; we expect the conductivity to be homogeneous over this length scale, and by staying larger than $\approx$50μm we avoid introducing the small-spacing errors discussed in section 3.1.2.2. Measurements at each probe spacing are taken at several different locations on the sample, taking care to position the probes as far as possible from sample edges. The variation in probe separation is randomized with respect to time, which eliminates the possibility of convolving temporal trends with probe spacing trends.

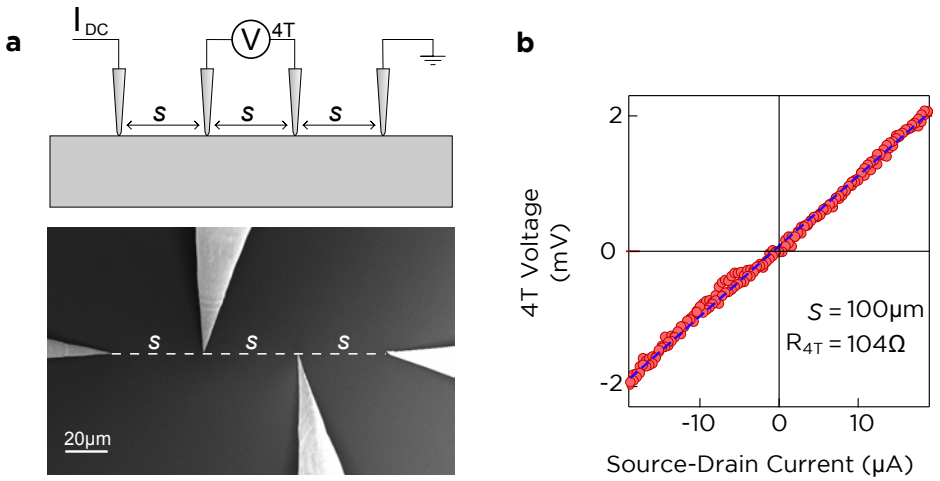


Figure 3.15: **The experimental method for a four-probe resistance measurement.** Under the observation of the SEM, the probes are positioned in a an equidistant, collinear configuration (a). The outer probes sweep a DC current while the inner probes record a potential difference. The gradient of such a V-I trace corresponds to a four-terminal resistance (b).

3.2.3.2 Experimental results

In Figure 3.16 we compare the probe spacing dependent four-probe resistance across three Si(100) substrates: 300 μm thick 1-10 Ωcm p-type, 300 μm thick 1-10 Ωcm n-type and 2 μm thick 5 Ωcm p-type silicon-on-insulator (SOI). These have been chosen in order to vary both the substrate doping type (p vs. n) and dimensionality (bulk vs. SOI). In each case the data has been taken from several different samples to ensure reproducibility.

The bulk p-type samples in Figure 3.16a show a resistance inversely proportional to the probe spacing, as expected from Equation 3.1. To fit the data we use a modified form of Equation 3.1 which includes the finite depth correction factor $F1$, since the largest spacing (250 μm) is comparable to the sample depth (300 μm). Fitting yields a resistivity of (6.7 $\pm$1.5) Ωcm, in agreement with the nominal doping range of 1-10 Ωcm. The uncertainty of $\pm$1.5 Ωcm represents the minimum range of values which will entirely encompass the measured data, as indicated by the shaded region in Figure 3.16a.

Despite having a comparable doping density the bulk n-type samples (Fig 3.16b) demonstrate very different behaviour, with much higher resistance values that are independent of probe spacing. As has been previously reported[81;96], this is due to the presence of a high resistivity inversion layer, a consequence of Fermi level pinning at the silicon surface. In the case of 2$\times$1 reconstructed Si(100), photoemission measurements have demonstrated that the Fermi level is pinned at $\approx$0.34eV above the valence band edge by surface states[97;98].

The consequence of this effect is that n-type substrates form a thin, high resistivity inversion layer at the surface, as depicted in Figure 3.17a. Here we have used a 1D Poisson

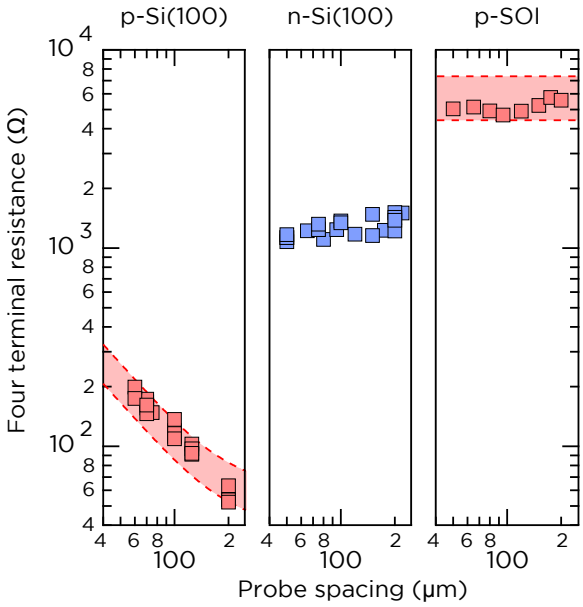


Figure 3.16: **Influence of the substrate type on four-probe resistance measurements** Resistance measurements performed as a function of probe separation on three different silicon substrates. In each case a clear signature of the substrate type is obtained, as discussed in the text.

solver[99] to evaluate the band-bending at the surface for a 7 Ωcm n-type substrate with a surface Fermi level pinned at 0.34 eV above the valence band maximum. An inversion layer ≈200 nm thick results, with an average free carrier density 2 orders of magnitude lower than in the bulk. This effectively isolates the bulk substrate, and conduction occurs only through the thin, resistive inversion layer. The presence of this inversion layer can be confirmed by examining single probe tip-sample measurements as in the preceding section. In Figure 3.17b we see that both n-type and p-type samples have rectifying I-V characteristics, but anomalously the rectification is in the same direction for both substrate types. High conductance when the tip is negatively biased with respect to the sample corresponds to a p-type substrate, as shown schematically in Figure 3.18. The implication is that in the vicinity of the probe contact the n-type sample is inverted to p-type, in agreement with our expectations from the simulations in Figure 3.17a.

Problems caused by this effect are unique to microscopic 4 probe systems, since more conventional macroscopic systems employ a much higher contacting load. The high pressure causes a local metallic phase transition in the silicon as discussed in section 3.2.2, resulting in Ohmic contacts underneath the probes. In addition, the large contact loading causes observable deeper penetration of the probes into the substrate, reaching through the surface inversion layer. In addition, In Figure 3.19 we show electron microscope images of a silicon substrate after making a measurement with a standard *ex situ* 4 probe system (i.e. not the Nanoprobe system we use throughout this thesis). This *ex situ* system

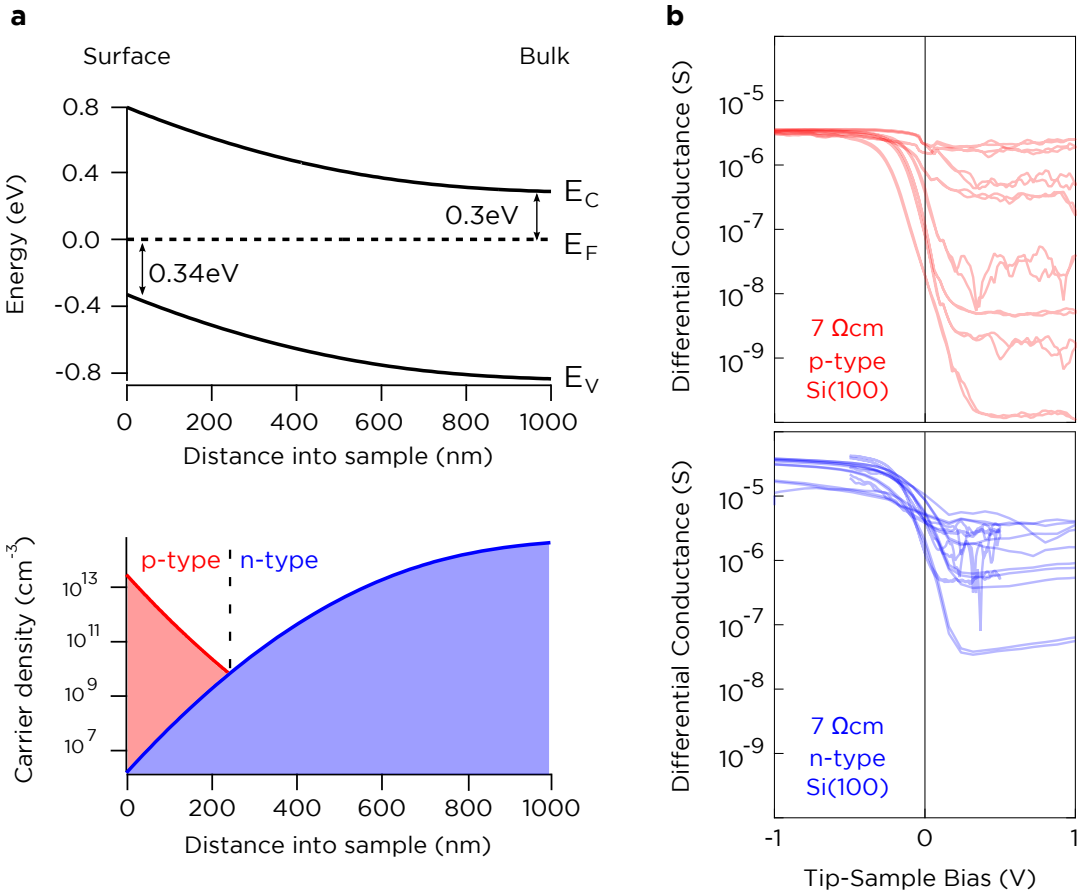


Figure 3.17: **Surface inversion layer as an explanation for unusual measurements on n-type substrates** The Si(100) 2×1 surface has a surface Fermi level pinned at ≈0.34 eV above the valence band maximum, which results in significant band bending and a surface inversion layer for n-type substrates (a). The presence of a p-type inversion layer is supported by single-probe I-V measurements (b), which demonstrate that both n- and p-type substrates rectify in the same direction. (*Poisson modeling performed with the Snider package*[99])

uses tungsten carbide probes with 100 μm radius probes, applying 100 g of loading force to the sample. From examining the abrasion and cratering left on the silicon surface, it is clear that this standard four-probe instrument will not be impeded by an inversion layer in the top 100-200 nm of the sample.

Finally, returning to Figure 3.16, the p-type silicon-on-insulator sample (Fig. 3.16c) has a 2 μm thick device layer, which remains effectively two dimensional for the range of probe spacings used here. From this substrate we obtain a four-terminal resistance of ≈5 kΩ, independent of probe spacing and in agreement with that predicted from the nominal resistivity and thickness of the device layer (shown by the shaded region).

We have now demonstrated that we can correctly interpret probe-spacing dependent resistance measurements of several different substrates. This understanding forms an

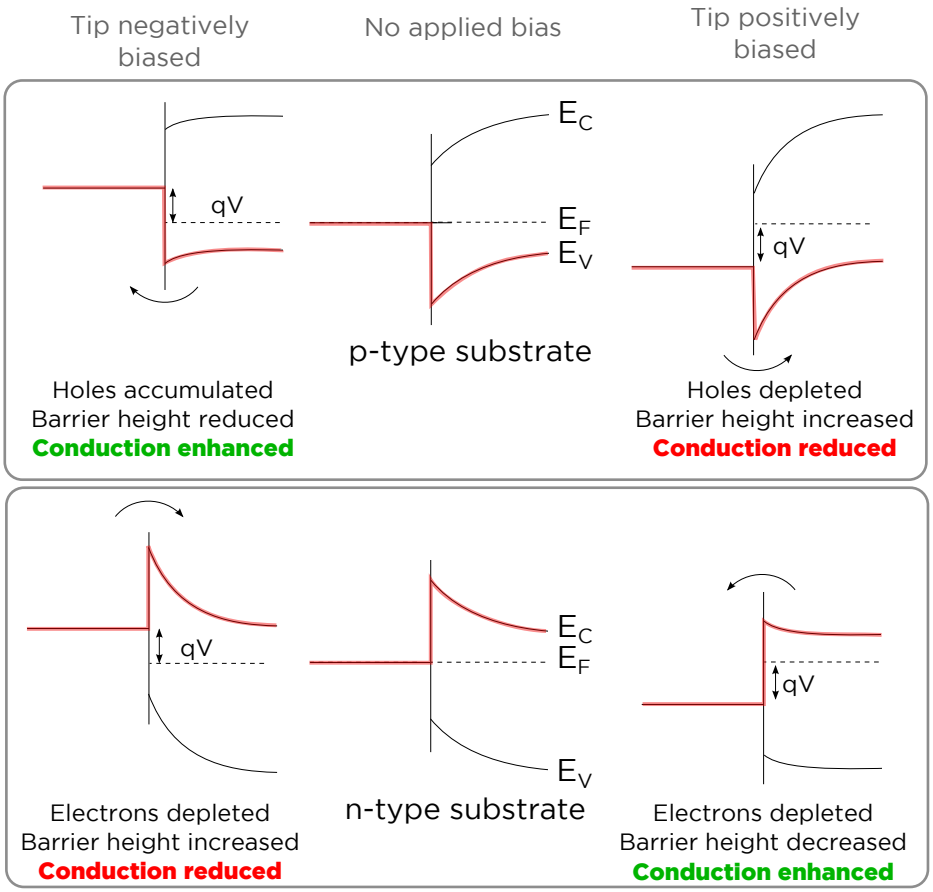


Figure 3.18: **Current rectification at a Schottky barrier** A schematic explaining the different rectification behaviour for p- and n-type substrates. The fact that we *do not* observe this opposite rectification behaviour in Figure 3.17b confirms the presence of a surface inversion layer in n-type samples, depicted in 3.17a.

important foundation for the later measurements where we δ-dope these substrates with phosphorus donors.

3.2.4 Temperature dependence of resistivity

The final experiments we will describe for the bare substrates are measurements of the temperature dependence of resistivity. An understanding of how the substrate alone behaves is crucial for interpreting the temperature-dependence of more complicated samples. It will also be useful to determine whether we can reach a sufficiently low temperature with the Nanoprobe system to 'freeze out' the background dopants in the substrate; this would then allow us to easily measure metallic structures on the surface without being concerned about parallel substrate transport.

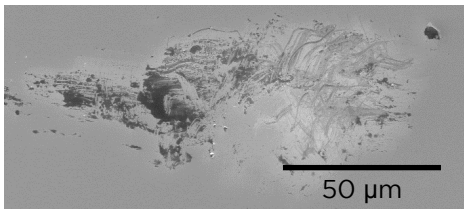


Figure 3.19: **Damage caused by a conventional 4-probe station.** An SEM image of a silicon surface after making a measurement with a conventional 4-probe system from Jandel Engineering. The large scale damage and depth of penetration make it clear why such systems are not sensitive to surface effects such as inversion layers.

3.2.4.1 Expected trends in resistivity with temperature

Before presenting measurement results, it will be useful to first discuss what trends we expect to see. The bulk resistivity of a semiconductor is a function of how many charge carriers are present (i.e. the carrier density, N_S) and how mobile those carriers are when subjected to an electric field (i.e. the mobility μ):

$$\rho = \frac{1}{q\mu N_S}$$

Carrier mobility in semiconductors is discussed by Ziman[100], and the specific case of bulk doped silicon has been comprehensively reviewed by Jacobini *et al*[101]. Mobility in bulk doped silicon is chiefly determined by contributions from:

- Ionized impurity scattering ($\mu \propto \mathrm{T}^{3/2}$)
- Acoustic lattice phonons leading to intra-band scattering ($\mu \propto \mathrm{T}^{-3/2}$)
- Optical lattice phonons leading to inter-band scattering (Complicated T dependence

Due to the combined influence of all three contributions, and in particular the complexity of inter-valley scattering, it is common to use phenomenological expressions which closely approximate measured data. Simple power law expressions of $\mu \propto \mathrm{T}^{-2.42}$ for electrons and $\mu \propto \mathrm{T}^{-2.20}$ for holes have been shown to provide excellent agreement for temperatures above ≈50 K and moderate doping densities[101]. In Figure 3.20a we show an example calculation of this behaviour for p-type silicon with a room temperature mobility of 450 $\mathrm{cm^2V^{-1}s^{-2}}$. The net effect is that as the temperature is lowered, the changes in mobility cause the sample resistivity to *decrease*.

The free carrier density is primarily determined by the degree of thermal activation into a conduction band. In the absence of extrinsic dopants, it is the ≈1.1 eV bulk bandgap which must be overcome, making the intrinsic carrier density nearly irrelevant around room temperature ($\mathrm{k}_B\mathrm{T}$=25 meV). Impurity doping introduces carriers much closer to the

band edges (≈50 meV), and it is these extrinsic carriers which constitute essentially the entire free carrier density for temperatures below ≈500K. At temperatures below ≈100 K there is insufficient thermal energy to completely ionize extrinsic dopants, and the free carrier density begins to sharply decrease. The net effect is that as the temperature is lowered, the changes in free carrier density cause the sample resistivity to *increase*. This is the opposite of the carrier mobility behaviour, but as thermal activation is an exponential process while the mobility follows a power law, at sufficiently low temperatures the incomplete ionization dominates and the substrate is said to be 'frozen out' into an electrically insulating state.

It is useful to model this behaviour in order to anticipate the temperature required to achieve substrate freezeout. The free carrier density for a given temperature can be numerically calculated following the graphical technique discussed by Van Zeghbroeck[102]. For a doped semiconductor in equilibrium, charge neutrality requires that the total density of negative charge (electrons and ionized acceptors) must equal the total density of positive charge (holes and ionized donors). Given the temperature, semiconductor bandgap, doping densities and dopant ionization energies we can compute all of these densities in terms of the Fermi energy:

$$\text{Ionized donor density} = \frac{N_d}{1 + \left(2e^{\frac{E_F-(E_G-E_A)}{kT}}\right)}$$

$$\text{Ionized acceptor density} = \frac{N_a}{1 + \left(4e^{\frac{E_A-E_F}{kT}}\right)}$$

$$\text{Electron density} = 2\left(\frac{2\pi m_0 m^* kT}{h^2}\right)^{\frac{3}{2}} e^{\frac{E_F-E_C}{kT}}$$

$$\text{Hole density} = 2\left(\frac{2\pi m_0 m^* kT}{h^2}\right)^{\frac{3}{2}} e^{\frac{-E_F}{kT}}$$

Where N_d andN_a are the extrinsic doping densities, E_G the bandgap and E_A the dopant ionization energy. The effective masses here are those for density of states calculations (1.08 for electrons, 0.81 for holes[102]). These expressions are valid in the non-degenerate limit where $E_f < 3kT$.

The calculation method involves plotting all of these equations as a function of Fermi level in the semiconductor; the physically correct value for the Fermi energy (and hence free carrier density) is that which satisfies charge neutrality. We will apply this model shortly when discussing experimental data, but in Figure 3.20b we plot an example curve for silicon doped to 2×10^{15}cm^{-3} with boron *. This is the most common doping level for the substrates used in our temperature dependence measurements, but it is worth noting that the temperature of the freezeout turndown in these curves is related more to the ion-

*The implementation of this method as an Igor Pro script is contained in Appendix B

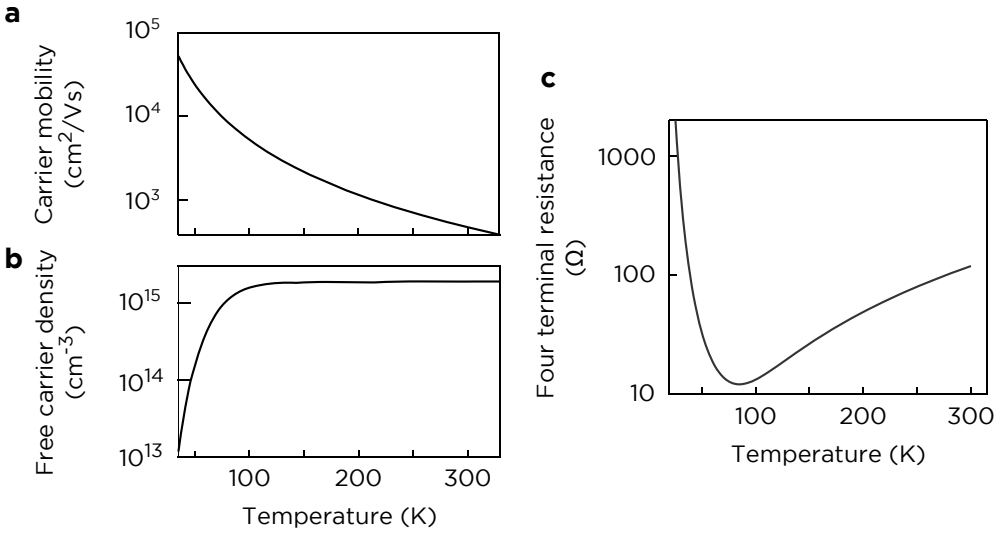


Figure 3.20: **Expected temperature dependence of a lightly doped bulk substrate** As described in the text, carrier mobility increases as the sample is cooled (a) while the free carrier density rapidly decreases below 100 K (b). The combined effect on resistivity is shown in (c).

ization energy of the dopant than to the doping density. The combined effect of mobility and free carrier density on the measured resistance is shown in Figure 3.20c. Having established what we *expect* to see, we have a basis for interpreting the experimental *in situ* four-probe measurements we show next.

3.2.4.2 Experimental method

The Omicron Nanoprobe system is equipped with a liquid helium flow cryostat, enabling cooling of the sample stage to ≈30 K, while a Pt100 resistor integrated into the stage provides reliable readout of the stage temperature. The chief experimental difficulty in making low-temperature measurements is that only the sample stage is cooled; the probes remain at room temperature. Maintaining electrical contact to the surface is difficult in the presence of such a temperature gradient. The tungsten probes contract when cooled (thermal expansion coefficient of 4.5×10^{-6} K^{-1}), causing them to pull back from the sample and break contact. As a coarse estimate, if the lower 500 μm of the probe cools by 50 K it will contract by 110 nm. When all four probes are doing this simultaneously, it becomes challenging to keep them in contact with the sample long enough to take a measurement. This can be overcome by manually keeping the probes in contact with the cold surface for long enough that they reach thermal equilibrium (essentially cooling the probes with the sample).

For this reason, the measurement technique adopted in this thesis for temperature dependence measurements is to establish this thermal equilibrium and then leave the probes on the sample surface, continuously sweeping the source-drain current and mea-

suring the four-terminal voltage. The stage temperature is swept sufficiently slowly that each up-down current sweep (and hence four-terminal resistance) can be assigned to a single temperature value.

Previously we discussed difficulties in measuring n-type substrates at room temperature due to the resistive surface inversion layer. For this reason we have focused our temperature dependence measurements on p-type substrates.

3.2.4.3 Temperature dependent resistance measurements of bulk p-Si(100)

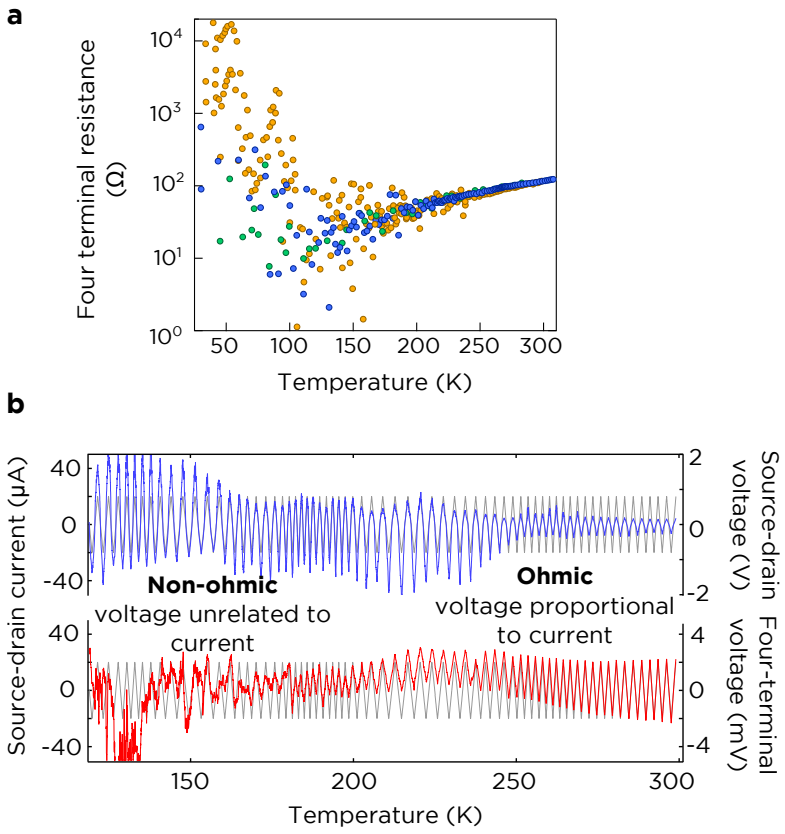


Figure 3.21: **Temperature dependent resistance measurements on p-Si(100) substrates.** Measurements on p-Si(100) substrates as a function of temperature (a) *appear* to show a freezeout-like increase in resistivity for temperatures below ≈150 K. However closer inspection of the data (b) reveals a gradual transition to non-Ohmic behaviour, questioning the validity of (a) and necessitating a different approach to the data analysis.

In Figure 3.21a we show four-probe resistance measurements from 3 different experimental data sets, each using a p-type substrate from the same 1-10 Ωcm Si(100) wafer. In all cases the temperature has started cold and been swept towards room temperature, with a probe spacing of 100 μm. At first glance it appears that we are seeing the substrate freeze out below ≈150 K, but inspection of the raw data indicates otherwise. In Figure 3.21b we plot in gray the source-drain current being swept up and down as the temper-

ature increases. Superimposed we show the two-terminal voltage required to produce this current (blue) and the measured four-terminal voltage (red).

Over the full temperature range the two terminal voltage and current remain well coupled, which indicates that the substrate has not frozen out (in Figure 3.21b this would manifest as the source-drain voltage diverging to tens of volts). However below ≈150 K the four-terminal voltage becomes decoupled from the source-drain current, and it becomes steadily less meaningful to evaluate a four terminal resistance from a linear fit to the data. This behaviour (or 'poorness of fit') can be quantified by examining the Pearson's coefficient of determination[103]:

$$r^2 = 1 - \left(\frac{\sum (y_{fit} - y)^2}{\sum (y - y_{avg})^2} \right)$$

This quantity describes how well a data set is represented by a least squares linear fit, where $r^2 = 1$ indicates that the data set is completely explained by a linear fit, while $r^2 = 0$ indicates that the fit is no better than a constant. In Figure 3.22 we plot the r^2 values for the data sets making up Figure 3.21a, together with examples of increasing poor fits.

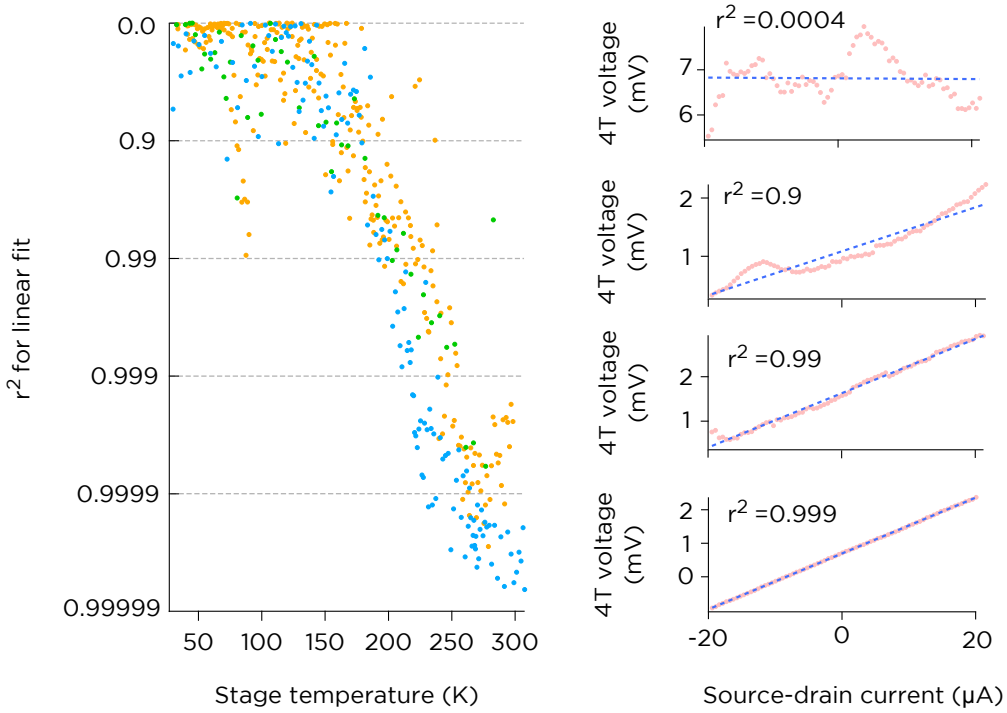


Figure 3.22: **Correlation analysis of the temperature dependence data.** A plot of Pearson's r^2 parameter for the data in Figure 3.21a clearly demonstrates what was qualitatively observed in Figure 3.21b: as the temperature is decreased, the four-terminal voltage becomes increasingly less correlated with the source-drain current. Example traces are shown for a range of r^2 values, from which it is clear that at the lowest temperatures a linear fit of the V-I trace is meaningless.

If we filter out all traces with $r^2 < 0.9$, we obtain the revised plot in Figure 3.23. In Figure 3.23b we plot the remaining data points together with a theoretical resistance curve encompassing both the $T^{-2.2}$ dependence of mobility and the numerically computed temperature dependence of carrier density (discussed in section 3.2.4.1). Inputs for this model are the activation energy of the boron dopants (E_A=46.25 meV[104]), a room temperature mobility of 450 $cm^2V^{-1}s^{-2}$[101] and doping density of 1.86×10^{15} cm^{-3} (based on the mobility and a room temperature resistivity of 7 Ωcm (Figure 3.16)).

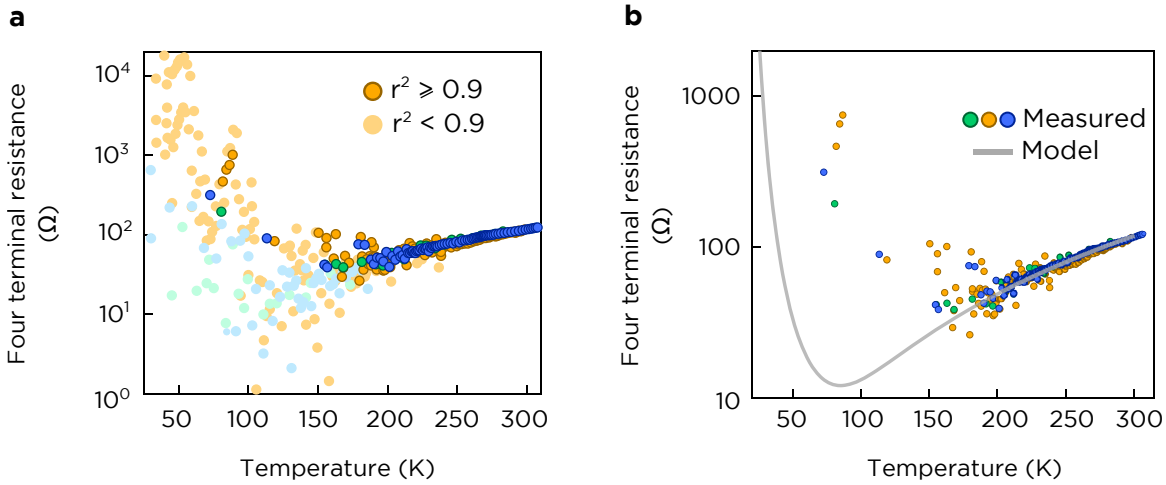


Figure 3.23: **Temperature dependent resistance measurements on p-Si(100) substrates, filtered by r^2** (a) The data set from Figure 3.21, where V-I traces with $r^2 \leq 0.9$ have been filtered out. The remaining data together with the theoretical model for the substrate are plotted together in (b).

This theoretical model appears to adequately account for the measured data for temperatures above ≈170 K. In this range the temperature dependence is dominated by the improvement in mobility, and cooling the substrate *reduces* the resistivity. On the basis of this model we would not expect to see the effects of incomplete donor ionization until temperatures reach ≈80 K, with the resistance exceeding 100 times the room temperature value for T<22 K.

However the few valid data points below 150 K suggest that some manner of transition is occurring at higher temperatures than expected from the bulk model. Similar observations when measuring with microscopic four-point-probe systems have been made previously by Wells[82] and Matsuda[105]. Both explained this behaviour in terms of the evolving band-bending at the surface. In Figure 3.24 we show 1D Poisson simulations illustrating the emergence of a surface depletion layer in p-type Si(100) as the sample is cooled. The mechanism is similar to the inversion layer in n-type samples discussed earlier (Figure 3.17), only here it is the evolving *bulk* Fermi level which drives the surface band bending. What begins as a mild depletion region at room temperature (Figure 3.24a) becomes more severe as the bulk Fermi level moves towards the valence band

edge. While the deep bulk of the substrate remains conductive at this temperature, the upper 200 nm electrically isolates it from the measurement probes. This can account for both the increasing resistance seen in 3.23b and the gradual loss of correlation between the surface potential and source-drain which occurs at the same temperature. In the latter case, heavily biased source/drain probes current may be able to locally alter the band-bending and cause current to flow through the conductive bulk substrate, but the voltage probes remain decoupled and are insensitive to the underlying potential profile.

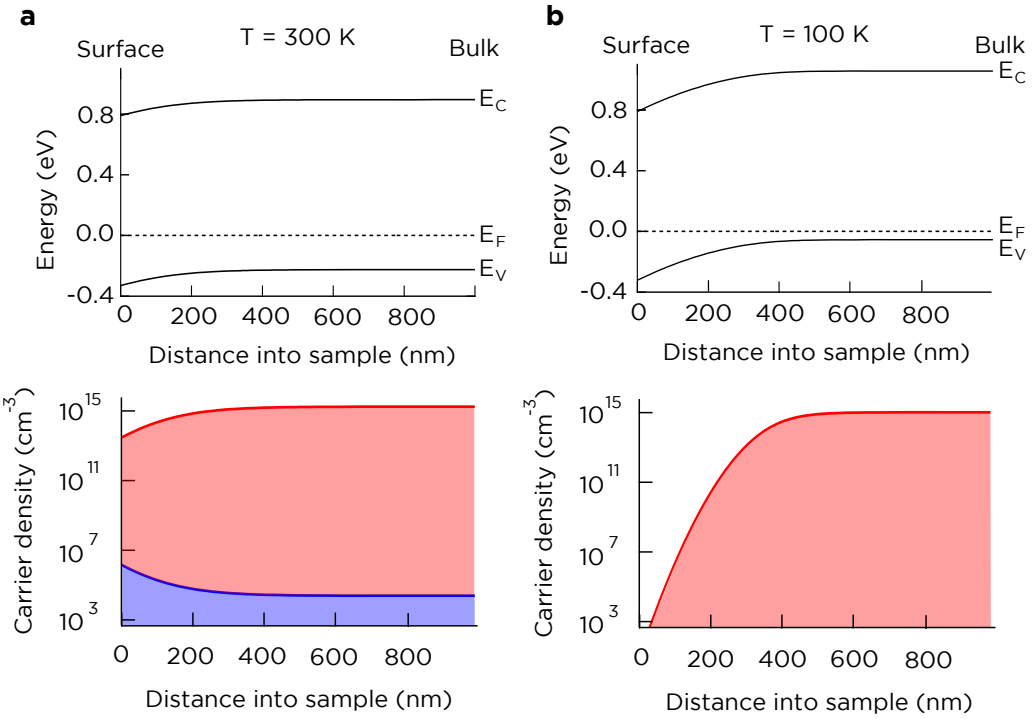


Figure 3.24: **Temperature dependent surface band bending in p-Si(100) substrates.** Changes in the surface band bending (driven by changes to the bulk Fermi level position) can account for the insulating transition occurring at ≈150 K. At room temperature (a) the surface is only weakly depleted, but by 100 K the depletion has become severe (b) (*Poisson modeling performed with the Snider package*[99]).

3.2.4.4 Outcomes

The motivation for performing low temperature measurements of bare substrates was twofold: we hoped to qualitatively understand the temperature dependence of resistance measurements, and also establish whether the Nanoprobe system would be capable of freezing out the substrate. The qualitative behaviour has been successfully identified: from room temperature to ≈150 K, an improving carrier mobility due to reduced phonon scattering events leads to a $T^{-2.2}$ dependence, in agreement with established empirical studies. Below 150 K, surface band bending creates a severe depletion layer at the surface, insulating the upper ≈200 nm from the rest of the substrate. In a sense this can

be considered a 'high temperature' freezeout, since it manifests ≈100 K before incomplete dopant ionization renders the entire substrate insulating. However this mode of substrate freezeout is not useful for unambiguously characterizing surface features or doping layers. This is because the effect we see here is dependent on near-surface band bending, and can easily be destroyed by altering the surface Fermi-level pinning. Conventional bulk freezeout (i.e. incomplete dopant ionization) is more robust in this sense, as it is not affected by changes to the silicon surface. However our numerical simulations indicate that for the substrates in use here, conventional freezeout requires temperatures of less than ≈22 K, which is below the minimum achievable sample temperature in the Nanoprobe system (≈30 K).

3.3 Electrical active delta-layers

Having characterized and understood measurements on a bare substrate, we now proceed to phosphine δ-dope the sample and examine the effect that this has on both single probe I-V curves and four-probe resistance measurements as a function of probe spacing. We will see that these measurements give a strong indication that the δ-layer has formed a 2D conduction path which now dominates the transport behaviour of the sample.

3.3.1 Experimental method

The process of δ-doping with silicon was described in detail in the opening section of chapter 1. Here we will briefly review this process and provide more specific experimental details of how the process is realized in the Nanoprobe system.

A clean Si(100) 2×1 surface reconstruction is the starting point, and is obtained by an annealing sequence in UHV as described in the preceding section. After allowing ≈5-10 minutes for the chamber pressure to recover and for the sample to cool to room temperature, high purity phosphine gas is introduced to the chamber. A chamber pressure of 5×10^{-9} mBar is maintained for 5 minutes, equivalent to a dose 1.4 L of phosphine. This leaves the silicon surface terminated with a monolayer of phosphine fragments (PH_x). A short annealing step (350°C for 60 s by direct heating) causes the phosphorus atoms to substitutionally incorporate into the top layer of the silicon lattice. To complete the crystalline environment for the phosphorus atoms, the sample is then reduced to a temperature of 250°C and epitaxially overgrown with silicon. For this we employ a commercial silicon sublimation source, the SUSI-63 from MBE Komponenten. This consists of a high resistivity silicon filament (float-zone, $\rho > 1$ kΩcm), which when raised to ≈1200°C by direct current heating produces a stable silicon flux at very low growth rates of ≈ 3 Å/min.

A schematic of the resulting structure for a 4 nm overgrowth is shown in Figure 3.25. The choice of growth parameters described has been shown previously to optimize the electrical properties of the layer[106] while minimizing dopant segregation and diffusion[107]. We will discuss both segregation and diffusion in detail in the following chapter; for the present purposes it is not essential that we precisely know the width of the doping profile. With 25 nm of encapsulation this process is known to result in full dopant activation with very high 2D carrier densities of 2×10^{14}cm^{-2}. In this chapter we will focus on samples with an encapsulation thickness of ≈4 nm, and in the next we will address how the electrical properties evolve as a function of encapsulation thickness.

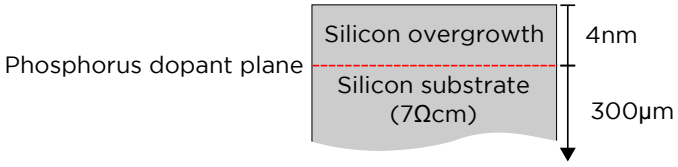


Figure 3.25: **Schematic of the δ-doped sample structure** After incorporating a monolayer of phosphorus dopants on the substrate surface, the sample is epitaxially overgrown with a few nanometers of high resistivity silicon.

3.3.2 I-V characteristics

In section 3.2.2 we discussed single probe I-V measurements on the undosed substrates. We found that the current in such measurements can either be dominated by the rectifying metal-semiconductor contact, shunt resistance or substrate resistance depending on the applied bias. As shown in Figure 3.26a there is a marked change in I-V measurements after δ-doping the sample and encapsulating with 4 nm of epitaxial silicon. The rectification appears to have been eliminated and the conductivity significantly increased. This is borne out by examining plots of $\ln(\frac{dI}{dV})$ versus V, shown in Figure 3.26b. Compared to similar plots before δ-doping (Figure 3.12) the forward bias conductance is 1-2 orders of magnitude higher. Some slight asymmetry can still be seen in some of the traces, but the *rectification ratio*, defined as (I at -200mV)/(I at +200mV), ranges from 0 to 3.5 whereas before δ-doping it ranged from 3 to 3×10^4.

Both of these observations can be understood in terms of the highly doped layer being introduced near the sample surface. In chapter 1 we noted that the effect of a δ-doping layer on a metal-semiconductor contact was to narrow the Schottky barrier, such that the dominant transport mechanism changes from thermionic emission *over* the barrier to quantum mechanical tunneling *through* the barrier. The latter process gives symmetrical conduction with respect to the applied bias, eliminating rectifying behavior. In this interpretation the remaining bias assymetry reflects the relatively small amount of current which is still attributable to thermionic emission. Once carriers have entered the sample,

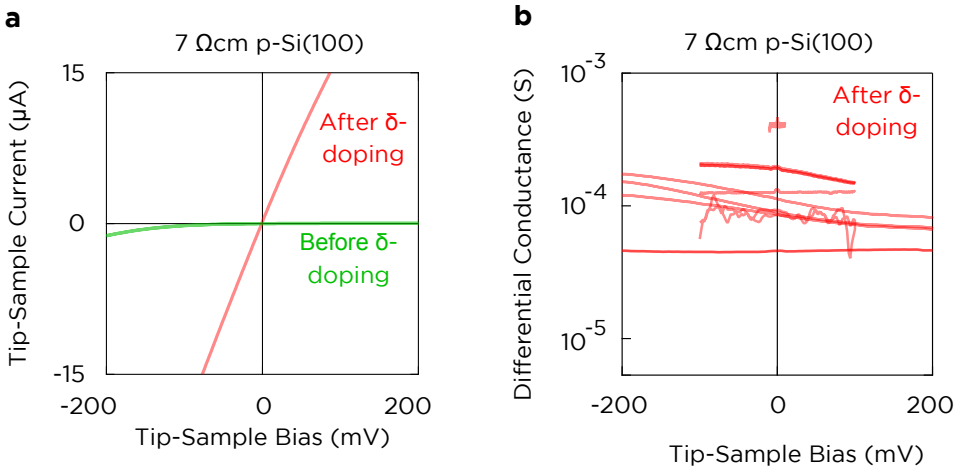


Figure 3.26: **Single probe current-voltage traces on 4nm deep δ-doped samples.** The current-voltage characteristics of a silicon sample are significantly changed after δ-doping (a), becoming Ohmic and significantly more conductive. This behaviour is highlighted by examining differential conductance traces for many different probe contacts (b). Compared to similar traces for the substrate alone (Figure 3.12) the rectification is nearly absent, and conductances are several orders of magnitude higher.

the overall conductance is greatly enhanced relative to the bulk doped substrates owing to the additional, highly conductive pathway through the δ-doping layer.

3.3.3 Probe spacing dependent four-terminal measurements

We now progress to the main aim of this chapter, four-terminal measurements of δ-doped silicon. Earlier in Figure 3.16 we showed probe-spacing dependent resistances for three different silicon substrate types: 300 μm thick 1-10 Ωcm p-type, 300 μm thick 1-10 Ωcm n-type and 2 μm thick 5 Ωcm p-type silicon-on-insulator (SOI). In Figure 3.27 we reproduce this data, but overlay the results of new measurements on these substrates after δ-doping and encapsulating with ≈4 nm of epitaxial silicon. Where previously the four-terminal resistances spanned two orders of magnitude across the three different substrate types, they now all converge to (310±60) Ω at all probe spacings. We note that for any single sample the resistance variation is typically better than ±20 Ω; in Figure 3.27 we have combined the results of many separate sample preparations, giving rise to a larger measurement variance.

That the measured resistance should now be independent of both the probe spacing and the properties of the underlying substrate provides a strong indication that conduction through the δ-layer dominates transport in all cases. If this is the case, we can use Equation 3.2 to extract a sheet resistance of ≈(1400±270) Ω/□. It is difficult to make a direct comparison between this value and that obtained from Hall bar measurements in chapter 1, since in that case the δ-layer was buried much deeper and the measurement was performed at cryogenic temperatures. A more equitable comparison may be made to

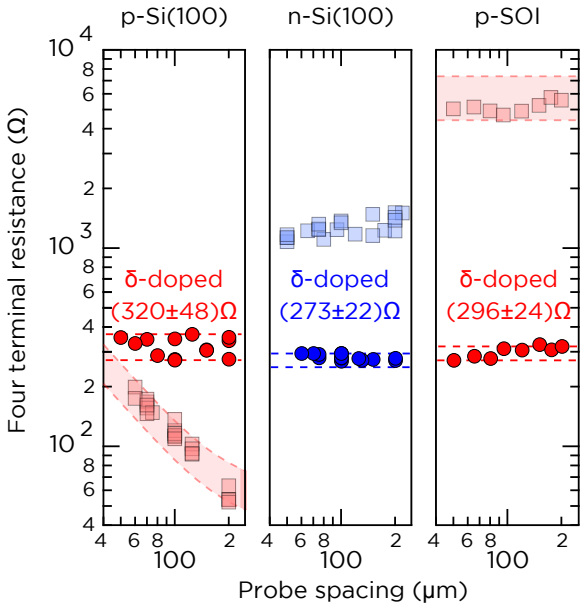


Figure 3.27: **Resistance measurements of δ-doped silicon.** Probe-spacing dependence of the four-probe resistance of three different silicon substrates, before (light squares; data from Figure 3.16) and after (dark circles) phosphorus δ-doping. For all samples the encapsulation thickness is (4.0±0.5)nm. Across all substrate types the resistance has converged to a spacing-independent resistance of (310±60) Ω.

the shallow samples of Clarke[108], which were fabricated in an identical manner to those discussed here but removed and measured *ex situ* as Hall bars at 4.2 K. At a nominal encapsulation depth of 4 nm a resistivity of 1096 Ω/□ was measured. Given that we expect the resistivity to be higher at room temperature due to phonon-scattering events, the ≈1400 Ω/□ we have obtained here seems to be an appropriate resistivity for a δ-layer.

It is not immediately apparent why the resistance measurements should be unaffected by parallel transport through the underlying conductive substrates. This is especially the case when we consider previously reported difficulties in measuring ultra-shallow p^+/n or n^+/p junction structures, where parallel transport through the substrate is a critical issue[109]. In particular, while the absence of leakage through p-type substrates can be rationalized by the formation of a p-n inversion layer, this cannot explain the measurements on n-type substrates where we have an n^+/n doping structure and would expect excellent electrical contact to the substrate.

In the following section we examine a number of independent indications that we are truly measuring the δ-layer exclusively, before finally offering an explanation for this result on the basis of *two-terminal* resistances.

3.4 Is conduction really through the δ-layer alone?

In the previous section we saw that the resistance measurements were independent of probe spacing, indicating that we were measuring a purely two-dimensional conduction path. We now provide additional evidence to support this point. In this section we will show that the measured transport is through a two-dimensional channel, and furthermore that this 2D channel can only be the δ-doping layer.

3.4.1 Two-terminal measurements

Whenever a four-terminal measurement is made, we simultaneously record the two-terminal voltage applied across the source and drain probes. As a stand-alone technique this is problematic due to the poorly controllable contact resistance - this is why four-terminal measurements are important. However while the lack of control means there is no limit to how *large* the two-terminal resistance can be, useful information is potentially conveyed by the *minimum* observed two-terminal resistance.

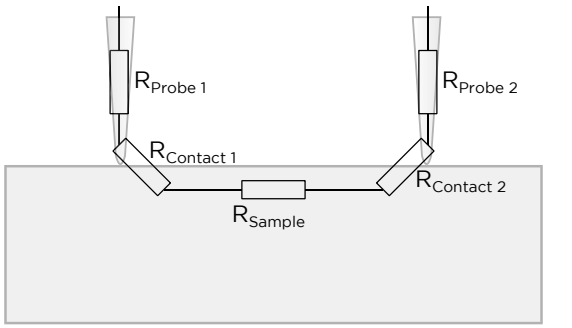


Figure 3.28: **The composition of two-terminal resistance for a homogeneous sample.** An equivalent circuit for a two-terminal probe-to-probe resistance measurement for homogeneous 2D or 3D transport.

To explain this, consider the components which contribute to a two-terminal resistance measurement of a homogeneous sample, such as pure bulk or pure δ-layer transport (schematically illustrated in figure 3.28). These components were discussed in detail in section 3.2.2. The lower bound for this total resistance corresponds to the case where the probe and contact resistances are negligible, leaving only the substrate resistance. The same Laplace derivations behind Equations 3.1 and 3.2 for the four terminal resistance can also be applied to obtain an expression for the substrate resistance. The derivation is

contained in Appendix A, but the results are:

$$\mathrm{R_{2T}} = \begin{cases} \frac{\rho}{\pi}\left(\frac{1}{r} - \frac{1}{d-r}\right) & \text{(3D)} \\ \frac{\rho_s}{\pi} ln\left(\frac{d-r}{r}\right) & \text{(2D)} \end{cases} \tag{3.12}$$

Where r is the probe contact radius, d the probe separation and ρ the sample resistivity. As an example, for a 7 Ωcm substrate with probes of contact radius 1μm positioned 300μm apart, we would expect this minimum resistance to be 22 kΩ [†]

Equation set 3.12 leaves us with the problem of needing to assume a resistivity. We can avoid this by also considering the simultaneously acquired four-terminal resistance. Combining Equation set 3.12 with Equations 3.1 and 3.2, we obtain:

$$\mathrm{R_{2T}} = \begin{cases} 2d\left(\frac{1}{r} - \frac{1}{d-r}\right) R_{4T} & \text{(3D)} \\ \frac{ln\left(\frac{d-r}{r}\right)}{ln(2)} R_{4T} & \text{(2D)} \end{cases} \tag{3.13}$$

For a given four-terminal resistance, these expressions provide us with the *minimum possible* two-terminal resistance for 2-dimensional and 3-dimensional transport, provided we know the probe separation d and radii r. Electron microscope observation provides us with a good estimate of both of these parameters. Making the assumption that transport occurs through either the substrate or the δ-layer but not both, this 'minimum observed resistance' offers an independent test of which layer is being measured.

In Figure 3.29 we plot experimentally obtained 2-terminal resistances against their corresponding, simultaneously acquired 4-terminal resistance. The measurements span several different δ-layer preparations, but in all cases are using an n-type 1-10 Ωcm substrate. Figure 3.29 encompasses samples where the phosphine dosing, annealing temperatures and overgrowth conditions have all been varied, resulting in four-terminal resistances spread over approximately an order of magnitude. For the present discussion the variation in four-terminal resistance is not important, we are simply interested in the relationship between the two- and four-terminal resistance. From Figure 3.29 we may make two observations. The first is that the scatter in two-terminal resistance is enormous; for a given four-terminal resistance the two-terminal measurements will typically span at least two orders of magnitude. This highlights the value of a four-terminal measurement technique. The second observation is that these two-terminal resistances are too low to correspond to transport through the bulk. Included in Figure 3.29 are dashed lines corresponding to the minimum possible values for bulk and δ-layer transport, calculated from Equation 3.13 using a probe separation of 100 μm and contact radius of 1 μm. It is apparent that the experimental data respects the theoretical minimum for 2D but not

[†]The inverse dependence on probe radius underlies the *spreading resistance profiling* technique for measuring resistivity - by using two probes with small contact radii the substrate resistance term can be made to dominate the contact resistance.

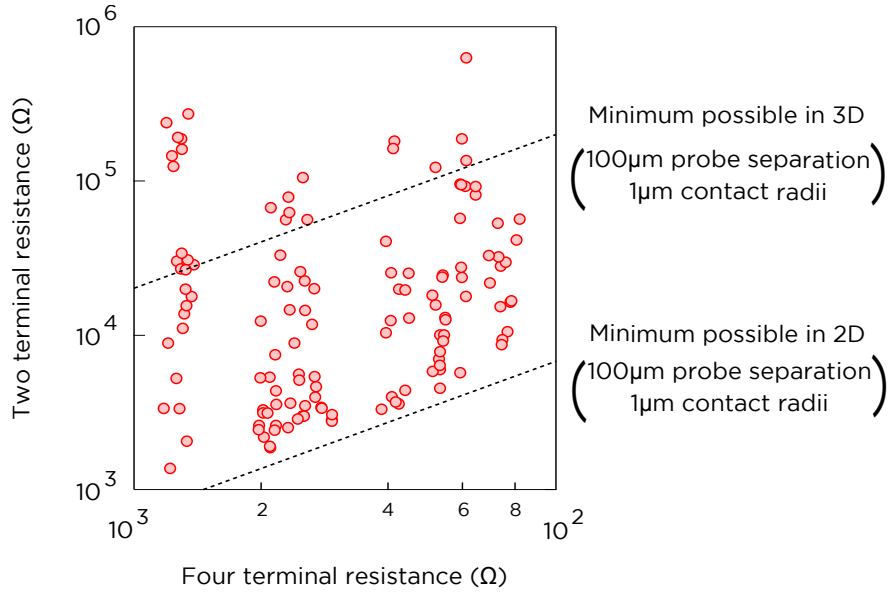


Figure 3.29: **The significance of the minimum observed two-terminal resistance.** Following the discussion in the text, each data point in this cumulative plot corresponds to a measurement of a four-terminal resistance and the simultaneously acquired two-terminal resistance. The theoretical minimum resistance of the δ-layer and bulk substrate (obtained from Eqn. 3.13) are plotted as dashed lines. The lower bound of the experimental data is too low to possibly correspond to bulk conduction, but agrees well with the lower bound expected from conduction through the δ-layer.

3D transport. Moreover, this result is not simply due to our choice of probe radius d or separation s. These values have been chosen as a reasonable 'worst case scenario' to demonstrate that no realistic choice of parameters could bring the 3D minimum in line with the measurements. (More typical values are d=300 μm, s<500 nm, in which case the 2D limit is still below the measured data but the 3D limit is even higher). This provides strong, independent evidence that the dominant transport path is not through the bulk substrate.

3.4.2 Other 2-dimensional aspects of the sample

So far we have demonstrated that we are measuring a two-dimensional layer, and that it is quite conductive (≈1.4 kΩ in Figure 3.27). Before we can conclude that this must be conduction through the δ-doping layer, there are two other possibilities to consider: the thin encapsulation layer and the semiconductor surface states.

3.4.2.1 Are we actually measuring the encapsulation layer?

The encapsulation layer for the phosphorus dopants in the preceding experiments has been a ≈4 nm thick layer of epitaxial silicon, grown from a high resistivity (>1 kΩcm) sublimation cell. If we make the assumption that the grown layer retains this very low

level of doping, it would possess a sheet resistance ρ/t of ≈2.5 GΩ/□, which is clearly too high to account for the ≈1 kΩ/□ we measure. However it is not obvious that the grown film should retain the low doping of the sublimation cell; it will almost certainly incorporate impurities from the vacuum background. Should these impurities act as dopants in silicon (atomic carbon and oxygen for example[110]), we may end up with a much higher conductivity overgrowth than anticipated.

To quantify this, consider that an n-type resistivity of 1 kΩcm corresponds to a doping density of ≈4×10^{12} cm^{-3} [102]. To retain the same resistivity in the 4 nm thick grown film, we must therefore maintain an areal doping density of 1.6×10^{6} cm^{-2}. This is a very small number, which can be put in context by making a simple calculation of the rate at which particles strike the surface during the growth. Using the kinetic theory of gases, it can be shown that this rate is:[32]

$$\frac{dN_s}{dt} \approx 2.7 \times 10^{21} \frac{P}{\sqrt{M}} \text{cm}^{-2}\text{s}^{-1}$$

where $\frac{dN_s}{dt}$ is the rate at which species strike the surface, P the background pressure in mBar and M the molecular weight of the species. The chamber pressure during silicon deposition typically reaches ≈3×10^{-10} mBar. If we assume for the moment a worst-case scenario where this pressure is entirely composed of atomic oxygen (M=16), this would correspond to roughly 3×10^{11} atoms per square centimeter striking the surface per second, or a total of 2×10^{14} strikes over the course of a 12 minute, 4 nm growth. At this rate, a sticking coefficient of only 1×10^{-8} would suffice to double the doping density (in reality oxygen has a sticking coefficient of ≈4×10^{-2} [111]).

There are too many unknowns to make a quantitative prediction based on this argument, rather we present it to highlight why we should not simply assume that the grown layer is as highly resistive as the source filament - experimental confirmation is necessary. To this end we have measured samples where we have grown a ≈4 nm silicon layer on a 1-10 Ωcm sample, *without* any phosphine doping. As shown in Figure 3.30, no change is observed compared to the substrate alone, with a constant four-terminal resistance of ≈1.5 kΩ that can be adequately explained by a surface inversion layer. It is clear that the encapsulation layer cannot be responsible for the ≈270 Ω observed when the sample is phosphine δ-doped.

3.4.2.2 Are we actually measuring surface-state conduction?

The second potential source of 2D conduction we should consider is the silicon surface itself. Semiconductor surfaces can possess metallic surface states which are directly conductive[96], or they can indirectly facilitate conduction by altering the near-surface band-bending within the substrate[112;113]. In the case of Si(100) there remains poor agreement in the literature, but the order of magnitudes quoted are typically MΩ/□ to GΩ/□[114;115]. Already we see that this conduction mechanism is far too poor to account for our mea-

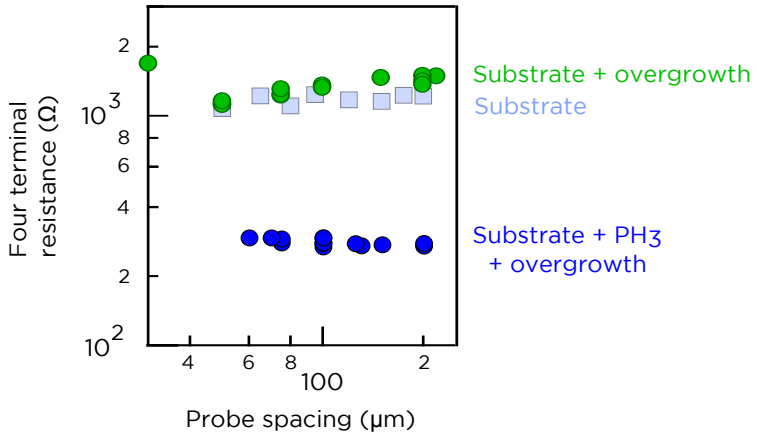


Figure 3.30: **A control study without phosphine dosing** To investigate whether it is the overgrowth itself that is conducting, we compare measurements on an n-type 1-10Ωcm substrate with and without the phosphine dosing stage. If the phosphine dose is skipped, the overgrown sample is unchanged from the starting substrate.

sured 1.4 kΩ/□

A simple experiment to conclusively make this point is to eliminate all surface states and see whether this has any effect. In Figure 3.31 we show the results of such an experiment, where we have fabricated and measured a δ-doped sample *in situ*, removed it to air for ≈24 hours and then reloaded it into UHV. Immediately prior to reloading the sample was chemically cleaned as described in section 3.2.1, including an HF treatment to remove the native oxide. Once back in UHV, without any further heating or cleaning treatments the sample was remeasured *in situ*.

This process is sufficient to completely destroy the clean silicon surface; within seconds of its removal the sample surface will be covered with water vapor and other atmospheric species, and over the 24 hour period will begin to develop a native oxide layer. Some caution is necessary for an experiment such as this; we wish to alter the surface alone, leaving the δ-doping layer unchanged. It has been shown previously that this condition is not satisfied for encapsulation depths of $\leq$8 nm. For this reason we have used an encapsulation depth of ≈20 nm. As a consequence of this thicker encapsulation, the four-terminal resistance is reduced: ≈130Ω instead of the 270 Ω we have seen previously with 4 nm encapsulation thicknesses. Again, this depth dependence effect will be fully investigated in the following chapter.

As can be clearly seen from Figure 3.31, eliminating the surface states has made very little difference to the electrical measurements. After exposure to air the resistance measurements have consistently increased by ≈3%, but it is clear that surface state conduction cannot be chiefly responsible for the 2D resistance observed in δ-doped samples. The 3% increase after exposure to air may be the result of a small surface conductance channel being removed, but could also readily be explained by a slight reduction in the encap-

sulation thickness. The surface oxidation which has occurred consumes silicon, slightly thinning the encapsulation layer.

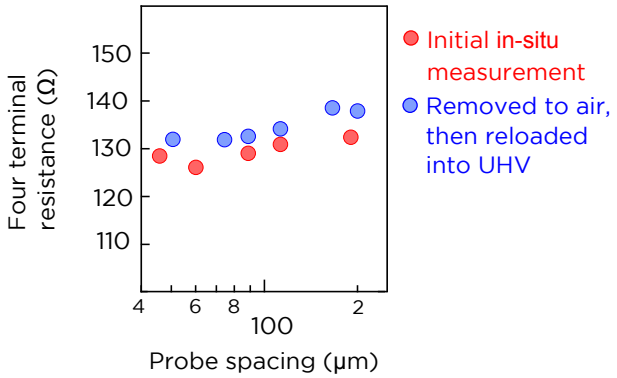


Figure 3.31: **Investigating the role of surface states.** The four-probe resistance of a δ-doped sample is not significantly changed by exposure to air, confirming that surface states are not responsible for the 2D conduction.

3.4.3 Temperature dependence of resistivity

We have now shown that after δ-doping, a 2D conduction channel appears which seems attributable only to conduction through the δ-layer itself. A completely independent test of this hypothesis can be obtained by examining the temperature dependence of the four-terminal resistance. This will also provide an indication of whether our measurements are still in some way influenced by the substrate.

In section 3.2.4 we showed that the substrate resistance could be well described by a carrier mobility following a $T^{-2.2}$ relationship for temperatures above ≈170 K. Below this temperature the upper ≈200 nm of the sample becomes highly resistive due to surface band-bending. What differences should we expect if this is truly a δ-doped layer that we are measuring? The doping in these layers is highly degenerate, such that the free carriers have extensive wavefunction overlap and form their own impurity band. As a consequence, these carriers cannot be frozen out at any temperature[102]. This impurity band also strongly pins the near-surface Fermi level close to the conduction band minimum, so we would not expect to see the same insulating transition exhibited by the substrate.

The temperature dependence of carrier mobility will also be very different[116]. Ionized impurity scattering will be strongly enhanced due to the concentration of free carriers in the same plane as their donor atoms. In addition, the close proximity of the surface will induce some degree of roughness scattering[117]. In the 30-300 K temperature range over which we have experimental access, phonon scattering will dominate. However the nature of the phonon scattering will differ from the bulk case, as the confined electrons in the δ-layer have a restricted range of available states to scatter into. The intra-subband

acoustic phonon scattering rate calculated for the 'extreme quantum limit' of a single occupied subband has a temperature dependence of $\mu \propto T^{-1}$, weaker than the $T^{3/2}$ for the bulk[118;119]. However calculations by Ryu[120] indicate that we are far from the single-subband limit in this structure, and hence should also consider inter-subband and inter-valley scattering. This greatly complicates modeling attempts, but experimentally it is found that under multiple subband occupation the mobility varies as $\mu \propto T^{-1}$ to $T^{-1.5}$[116].

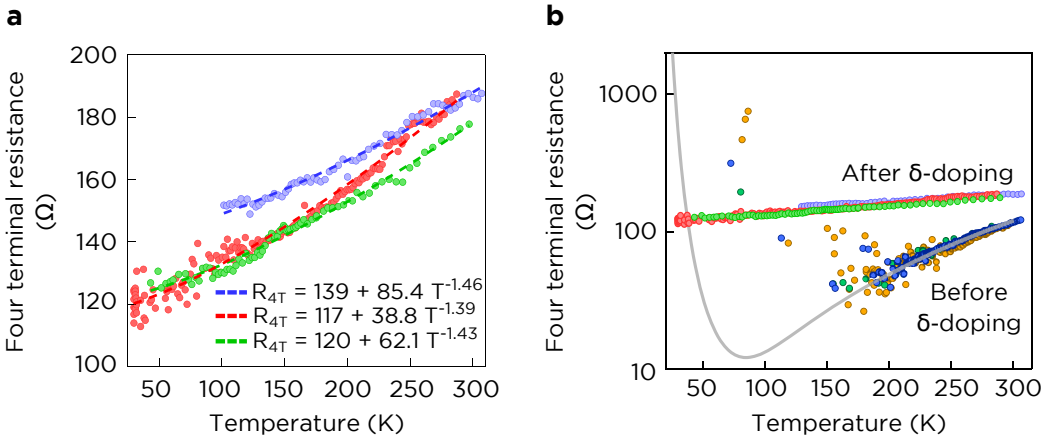


Figure 3.32: **Temperature dependent resistance measurements of δ-doped samples.** After δ-doping, the measured resistance exhibits the temperature dependence expected of a two-dimensional electron gas (a). No freezeout effect is observed over the accessible range, and the temperature dependence is significantly different from that of the substrate alone (b).

In Figure 3.32a we show four-probe resistance measurements for 3 separate (but nominally identical) preparations of a δ-doped n-type substrate. A slightly thicker encapsulation layer of 5-6 nm is used here which results in a lower room temperature resistivity than we saw in Figure 3.27b at only 4 nm depth [‡]. The measurement procedure is the same as for the substrate measurements described in section 3.2.4, where the probes are left on the cold sample surface while the temperature is gradually increased.

The data has been fitted with a power law of the form $R_{4T} = A + BT^{\gamma}$, in anticipation of a relationship of the form:

$$\begin{aligned} R_{4T} \propto \rho &= \frac{1}{qn\mu_{\text{effective}}} \\ &= \frac{1}{qn\mu_{\text{residual}}} + \frac{1}{qn\mu_{\text{phonon}}} \\ &= A + BT^{\gamma} \end{aligned}$$

Where the A term represents a 'residual' low temperature resistance and the BT^{γ} term

[‡]The reason for this reduction at deeper encapsulations will be explored in the next chapter

captures the effect of phonon scattering, such that we would should expect γ= 1 - 1.5 based on our preceding discussion. Figure 3.32a demonstrates that the data is well described by such an expression, with powers of 1.39 - 1.46 as expected for phonon scattering in a 2DEG. Importantly, this fit is valid over the full temperature range - if the room temperature measurement were a convolution of substrate and δ-layer conduction, we would expect to see a more complicated temperature dependence which reflects the different effects occurring in the substrate and δ-layer. This is further clarified in Figure 3.32b where we directly compare the temperature dependence of the δ-doped sample with that of a lightly doped substrate. It is clear that changes occurring in the substrate are not reflected in the δ-layer measurements.

3.4.4 What if conduction is through the δ-layer and the substrate in parallel?

We have so far been implicitly assuming an either/or scenario where transport is either entirely through the δ-layer or entirely through the substrate. Certainly all of the evidence so far suggests that we are seeing purely 2D conduction, but it seems plausible that *some* amount of current will be passing through the substrate. It is therefore worth taking a moment to discuss what to expect when there is mixed conduction, and specifically whether we would be able to detect it by performing probe spacing dependent resistance measurements.

The main difficulty in interpreting mixed conduction (i.e. simultaneous conduction through a 3D substrate and 2D overlayer) is that we surrender the condition of homogeneous resistivity, and analytical expressions for the potential distribution become difficult or impossible. Allowing for a *completely* arbitrary sample composition forfeits all symmetry and necessitates finite element numerical approaches[87]. However there are certain sample structures of practical importance where symmetry is only partially lost, such as a sample composed of layers of different resistivity material (i.e. piecewise homogeneous).

This 'multilayer' problem was first treated by Schumann and Gardener in the context of spreading resistance measurements[83]. Once an expression for the surface potential is obtained, the extension to an expected four-probe resistance is straightforward[121]. However the Schumann-Gardener expression is given in terms of an integral which must be numerically solved. A rigorous quantitative treatment of this approach is beyond the scope of this thesis, but we may make some simple qualitative observations. In the case of a two-layer system of a thin layer on a semi-infinite substrate (Figure 3.33a), we can apply the Schumann-Gardener model to obtain the following expression for the four-probe resistance:

$$R_{4PP} = \frac{2}{I}(V(s) - V(2s))$$

where I is the measurement current, s the equidistant probe spacing and $V(r)$ the surface

potential, given by:

$$V(r) = \frac{\rho_{top}}{\pi} \int_0^\infty \frac{sin(\lambda a)}{\lambda a} J_0(\lambda r) \frac{2ke^{2\lambda d}}{1 - ke^{-2\lambda d}} \mathrm{d}\lambda \tag{3.14}$$

with ρ_{top} the resistivity of the upper layer, d the thickness of the upper layer, a the radius of the current injecting contact and r the radial distance from the center of this contact. The parameter λ is simply an integration variable, while k is given by:

$$k = \frac{\rho_{\text{bottom}} - \rho_{\text{top}}}{\rho_{\text{bottom}} + \rho_{\text{top}}}$$

with ρ_{bottom} the resistivity of the substrate.

In Figure 3.33 we show the results of such calculations for representative 'regimes' of a two-layer sample such as that depicted in Fig. 3.33a:

- Scenario 1 (Fig. 3.33b): The bottom 3D layer is infinitely resistive ('pure' 2D conduction)
- Scenario 2 (Fig. 3.33b): The bottom 3D layer presents a minor leakage path (Mixed conduction, but 2D dominated)
- Scenario 3 (Fig. 3.33c): Both layers have identical resistivity ('pure' 3D conduction)
- Scenario 4 (Fig. 3.33c: The top 2D layer presents a minor leakage path (Mixed conduction, but 3D dominated)

The question we wish to address is this: if transport is a mixture of 2D & 3D, how will the four-probe resistance depend on probe spacing? Will mixed conduction cause sufficient deviation from the pure 2D (R_{4T}=constant) or pure 3D ($R_{4T} \propto \frac{1}{s}$) models that we would be able to detect it experimentally?

The dashed lines in Figure 3.33b and c represent the simple analytical models used so far in this chapter, while the solid data points correspond to simulations of mixed conduction as calculated with the Schumann-Gardener method (using the software package Maple to numerically integrate the first million terms of equation 3.14). We see that introducing mixed conduction does indeed result in a different functional dependence of resistance on probe spacing compared to the simple theoretical models. Figure 3.33b is particularly relevant to this chapter, and indicates that if the four-probe resistance has any downward curvature with respect to probe spacing then we should be suspicious about parallel substrate conduction. As can be verified by examining the data shown throughout this chapter, no such downward curvature is ever observed. This tells us that for the results we have presented so far, the simple analytical 'pure 2D' conduction model describes the data very well. We may safely assume that parallel substrate conduction, if occurring at all, is insignificant.

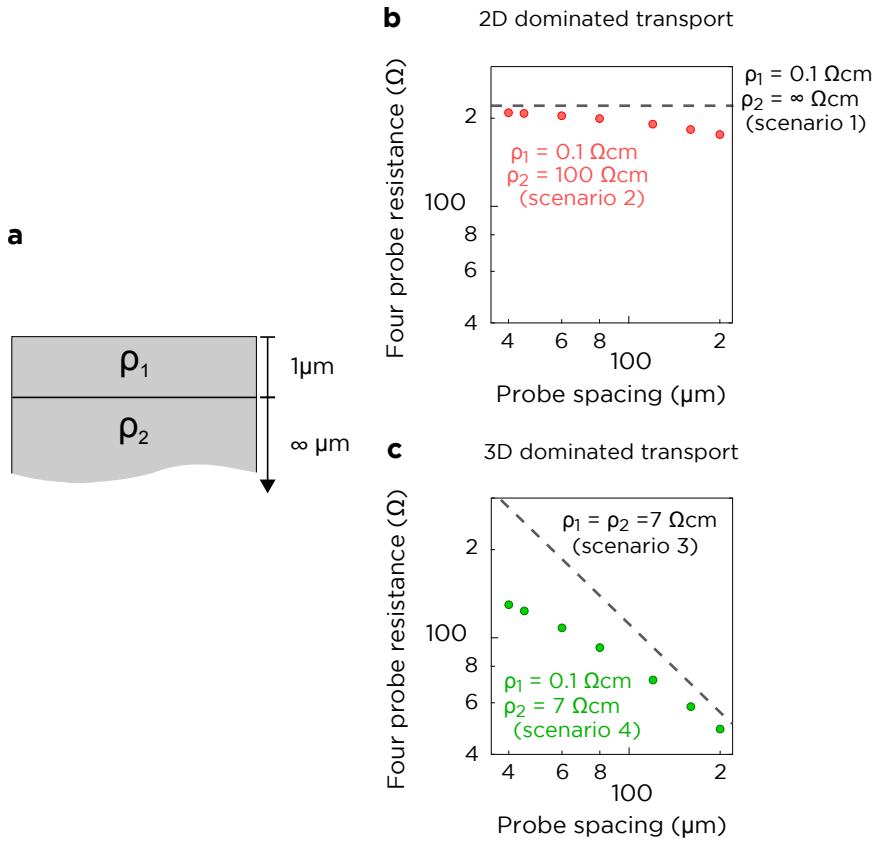


Figure 3.33: **Theoretical modeling of multi-layer conduction.** By employing the Schumann-Gardner method we can model the probe-spacing dependent four-probe resistance of a two-layer system such as that shown in (a). The solid lines in (b) and (c) depict the standard models we have been using for pure 2D (a) and 3D (c). The data points are calculated resistances for the case where conduction is through both layers, either 'leaking' through the substrate (b) or the surface layer (c). These calculations indicate that mixed conduction should be easily detected experimentally.

3.5 Why do we only observe conduction through the δ-layer?

At the end of section 3.3 we noted that we are most likely measuring transport through the δ-layer exclusively, which given the use of conductive substrates was an unexpected result. In section 3.4 we discussed further evidence to support this result, but the question of how this is happening remains unaddressed. In this section we will offer a model to account for the apparent electrical isolation of the δ-layer from the substrate.

In a multi-layered structure where two paths are in parallel, the ratio of their individual resistances will indicate the preferred current path. For example, if a 1 Ω resistor

is connected in parallel with a 10 Ω resistor, the smaller resistor will carry 90% of any electrical current. For our two-layer system of a δ-layer on a conductive substrate, it is misleading to use *four-terminal* resistances to evaluate this ratio, since it is the *two-terminal* resistance which determines the current distribution. This is an important conceptual point - typically a four terminal measurement allows us to completely ignore the nature of the current contacts, but in any circumstance where the current distribution is important we cannot abstract the current injection.

Thus we must consider the two-terminal resistances of the δ-doping layer and of the substrate. This was discussed in section 3.4.1, but we repeat the relevant equations here. For two probes contacting a semi-infinite 3D substrate, we have:

$$R_{2T} = \frac{\rho}{\pi}\left(\frac{1}{r} - \frac{1}{d-r}\right) \qquad \text{(3D)} \tag{3.15}$$

where r is the probe contact radius, d the probe separation and ρ the sample resistivity. For a semi-infinite 2D substrate, the equivalent expression is:

$$R_{2T} = \frac{\rho_s}{\pi} ln\left(\frac{d-r}{r}\right) \qquad \text{(2D)} \tag{3.16}$$

In Figure 3.34a we plot Equation 3.16 as a function of the probe radius for a 1 kΩ/□ 2D layer (green trace), with this resistivity corresponding to that of the δ-layer in Figure 3.27. We also plot similar traces for 3D substrates of different doping densities (130, 7 and 0.02 Ωcm). The two-terminal resistance increases as the measurement probes become sharper, since current close to the source or drain probes 'sees' an increasingly small volume (area) of the 3D (2D) layer. This effect is often termed 'spreading resistance', as discussed in section 3.4.1. Importantly, the increase in two-terminal resistance with decrease contact radius is much steeper for 3D substrates compared to the 2D δ-layer. As a consequence, for the ≈100 nm radius probes typically used in our experiments the δ-layer is ≈100 times more conductive than the 7 Ωcm bulk substrate it is created on, and hence the δ-layer dominates conduction.

To verify that this interpretation is correct we went on to perform similar δ-doping measurements using much higher (130 Ωcm) and lower (20 mΩcm) resistivity n-type substrates. If we consider the spreading resistance model in Figure 3.34a we would expect no change in the four-terminal resistance on a more resistive (130 Ωcm) substrate, since the δ-layer is now ≈1000 times more conductive than the substrate. However on the less resistive 20 mΩcm substrate the resistance ratio is reversed, with the bulk now 10-100 times more conductive than the δ-layer. In this limit we would thus expect four-probe measurements to revert to the bulk 3D relationship with probe spacing (Equation 3.1). Experimental data shown in Figure 3.34b matches these expectations. The light grey curves illustrate the expected four-terminal resistances of the substrate alone, while the

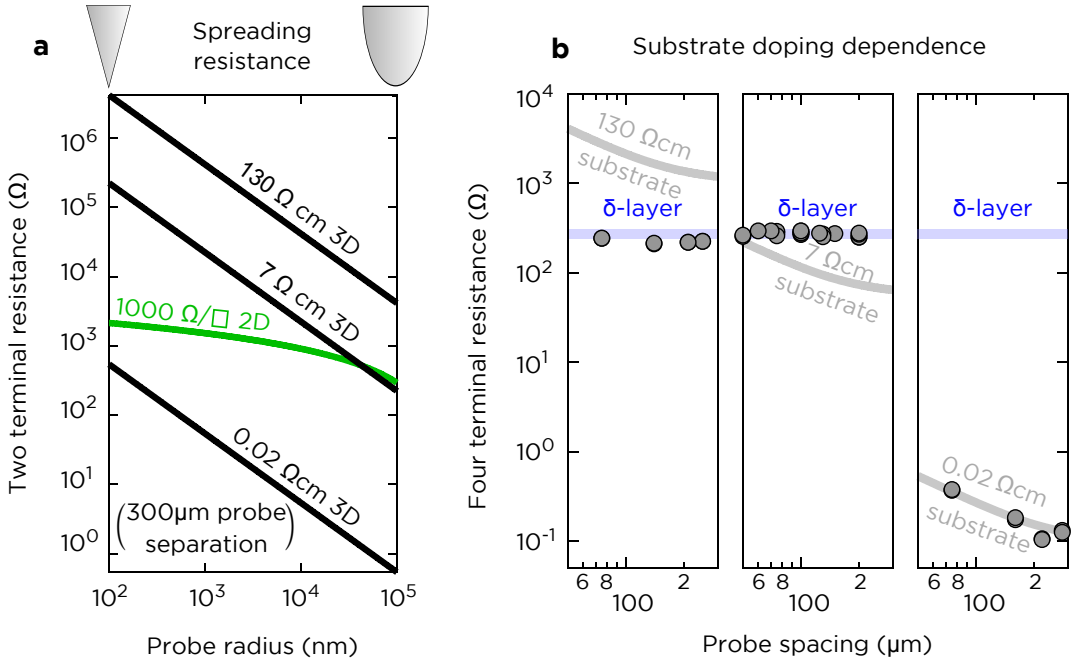


Figure 3.34: **The role of two-terminal resistance in bulk sensitivity** In (a) we show predicted (Eqns 3.15,3.16) two-terminal source-to-drain resistances as a function of probe radius for a variety of substrate doping levels. For the ≈100 nm radius probes used here, the 2D δ-layer (green trace) is ≈100× more conductive than an underlying bulk 7 Ωcm substrate. Experimental measurements of δ-layers on n-type substrates of different doping densities (b) confirm the predictions of (a). Four-terminal measurements are unchanged on a low doped (130 Ωcm) substrate, while bulk conduction dominates on a much heavier doped (20 mΩcm) substrate.

blue curves indicate the expected resistance of a 4 nm deep δ-layer as given by Figure 3.27. Measurements of 4 nm deep layers are unchanged when the substrate resistivity is increased from 7 to 130 Ωcm, while for the 20 mΩcm substrate bulk conduction dominates.

Thus we can attribute the lack of bulk sensitivity to three factors:

- The use of lightly doped substrates. Somewhere between 7 and 0.02 Ωcm substrate conduction becomes a problem, but since we have no reason to use samples of resistivity lower than 1-10 Ωcm this poses no problem.

- The extremely high doping density in the δ-layer, which presents a low-resistivity pathway for conduction.

- The use of nano-scale source/drain probes. As shown in Figure 3.34a, if we were to use conventional probes with a contact radius of >10 μm a much higher substrate doping density would be required to avoid significant parallel conduction.

3.6 Conclusions

In this chapter we have built up a comprehensive understanding of the application of an *in situ* four-point probe system for characterizing ≈4 nm deep phosphorus δ-doping layers in silicon at room temperature.

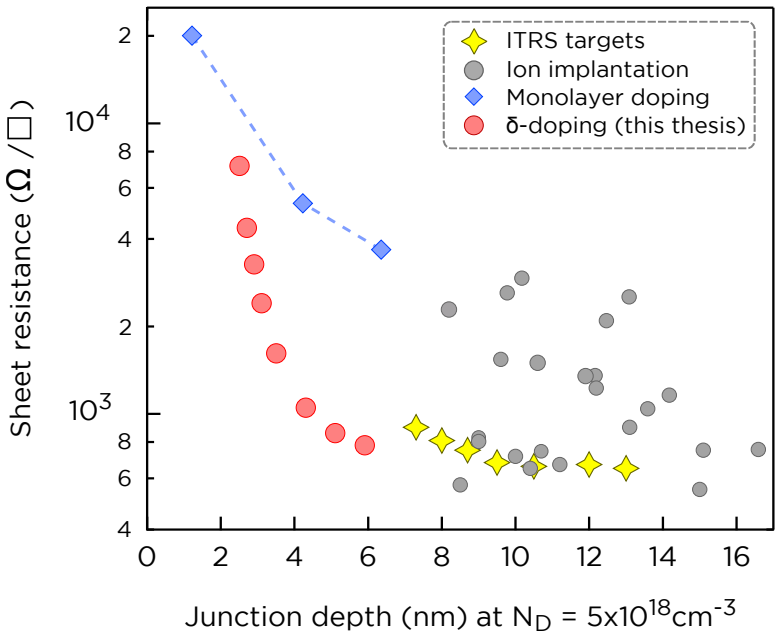
Since we could not avoid using conductive substrates, the major focus of the chapter was on proving that we could measure the resistivity of the δ-layer alone (and not a combination of the δ-layer and the substrate). To establish a frame of reference, we first studied a series of substrates alone (p-type bulk, n-type bulk and p-type SOI) and were able to account for all of our obervations on these samples. This included unusual behaviour due to surface depletion regions, which we found on n-type substrates at room temperature and p-type substrates at low temperature, both due to surface Fermi-level pinning.

Equipped with a good understanding of the substrates alone, we then characterized the more complicated δ-doped samples. These measurements gave the appearance of purely 2D conduction through the δ-layer (≈1.4 k$\Omega/\square$), uninfluenced by the conductive substrates. Through an exhaustive series of experiments measurements encompassing different substrate types and doping levels, different probe separations, temperature dependence and the elimination of surface states we were able to show that do indeed measure only the δ-layer. We could explain this in terms of the two-terminal spreading resistance to the 2D δ-layer compared with the 3D substrate, with measurements on different conductivity substrates supporting this explanation.

Prior to this work, any resistivity characterization technique (such as a low temperature Hall bar measurement) suitable for δ-doped layers involved removing the sample from UHV and potentially a delay of several days to fabricate surface contacts on the sample. In contrast, the four-probe measurements we have discussed here are made in *in situ*, do not permanently modify the sample and require only minutes to perform. This makes it appealing for systematic studies aiming to optimize sheet resistance, and in principle offers the ability to perform characterization part-way through a fabrication sequence. We will look at one such application in the following chapter.

In situ four-point probe systems are capable of many interesting applications beyond measuring sheet resistivities. In chapter 5 we will discuss some of these, concentrating on lithographically patterned dopant structures. Whilst in the present chapter we have been focused on measuring the resistivity of semi-infinite structures, the technical and experimental insights gained from this work will be an essential foundation for any future work.

The results of this chapter have been summarised in the Applied Physics Letters journal[80] and also presented at the 37th International Conference on Micro and Nano Engineering (MNE 2011) in Berlin.



The resistivity of near-surface Si:P δ-layers

Index of key results and discussions

Background information about ultra-shallow doping begins with section 4.1.1. For discussion and measurements of the physical dopant distribution in Si:P δ-doped layers, see section 4.2 on page 108.

Measurements of an incorporated PH3 dosed surface with no encapsulation layer are discussed in section 4.3.1. For measurements of Si:P δ-layers as a function of encapsulation thickness, see section 4.3.2 on page 113. These results are compared with industry targets and leading literature results on page 118. For discussion about how *electrically* wide a δ-layer is (i.e. carrier distribution), see section 4.3.4.

A model to explain the depth depdence trends is discussed in section 4.4. Specifically, the role of segregation is treated on page 122, surface scattering on page 124 and possible extensions to the model on page 128.

For discussion and measurements of very high doping density 'double dosed' δ-layers, see section 4.5 on page 130.

4.1 Introduction

In the previous chapter we investigated the applicability of an *in situ* four-probe system to characterize δ-doped Si:P samples. In this chapter we capitalize on the unique strengths of both the four-probe technique and the low temperature δ-doping technique by studying the evolution of δ-layer resistivities as a function of depth from the surface. In this section we begin by discussing the relevance and motivation for studying highly doped, near surface doping layers. To place our work in context, we also review existing methods to both create and characterize shallow doping layers.

4.1.1 Why shallow doping?

The concept of 'shallow doping', as we will use the term in this chapter, is to physically position dopant atoms as close as possible to the interface of a semiconductor without forfeiting their electrical characteristics as dopants*. There are several technological reasons for this being a worthwhile endeavour, but the largest and most immediately relevant of these comes from the microelectronics manufacturing industry. The astonishing progress in the price and performance of integrated circuits over the last few decades has been driven by a relentless push to reduce the geometric dimensions of transistors[122]. The shrinking of *lateral* dimensions is mainly a lithographic problem, but in the process we also encounter 'short channel effects' such as off-state leakage and threshold voltage shifts[123;124]. In order to mitigate these effects, doping technology capable of shallow, abrupt, highly conductive doping layers is required. The 2011 International Technology Roadmap for Semiconductors (ITRS) sets sub-8 nm depth targets by 2015[1], which is beyond the currently demonstrated limits of ion implantation techniques. There is therefore growing interest in alternative doping technologies to meet the needs of future semiconductor devices[79;113;125].

Looking beyond conventional computing architectures, shallow doping is also important for the rapidly developing field of quantum computation. Most donor-based solid-state quantum computer architectures involve being able to tune the properties of donors with surface gates (for example the 'A gates' in the Kane scheme to tune the hyperfine interaction[14]). In order to maximize the effect of these gates, the donors should be placed as close as possible to the surface. For this reason the study of donors close to interfaces is an area of active research[126;127].

Our aims in this chapter are to combine *in situ* four probe metrology with the low temperature Si:P δ-doping technique in order to answer two questions: Can Si:P δ-doping

*In the context of doping semiconductors, 'shallow' also commonly refers to the energy position of the dopant within the host bandgap, but throughout this chapter we will always mean spatially shallow.

constitute an interesting alternative to state of the art ultra-shallow junction (USJ) formation? For future quantum computing architectures, what can be said about the physics of these layers very close to the surface?

4.1.2 A definition of terms

Before we can meaningfully discuss shallow doping, we must define what we mean by 'shallow' and 'depth'. Conventional USJ literature defines *junction depth* to be the vertical distance from the silicon interface at which the physical doping density drops below 5×10^{18}cm^3, equivalent to the substrate background doping level (Figure 4.1a). Literature from the δ-doping community typically deals with sharp doping spikes, and the *width* (usually given as FWHM) of the spike is the preferred means of conveying the 'sharpness' of the doping profile. This is distinct from the *depth* of the δ-layer, which refers to the vertical depth from the interface to the centre of the δ spike. Ultimately both sets of terminology indicate the same property (the spatial distribution of free carriers in the sample), but care must be taken when drawing comparisons between the two approaches.

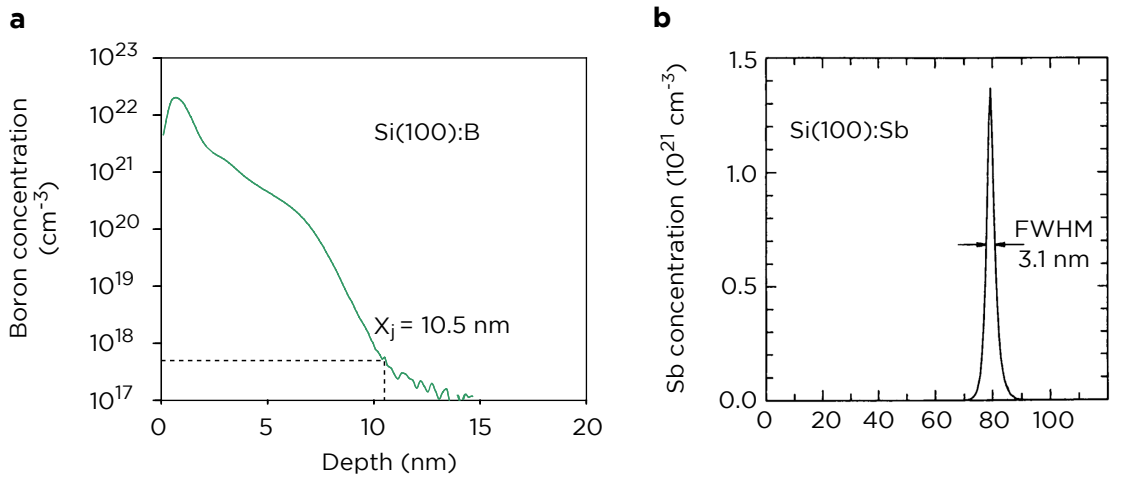


Figure 4.1: **Terminology associated with the description of doping profiles.** For conventional surface doping profiles (a) the profile width is described by the junction depth X_j, the distance at which the doping density falls below 5×10^{18}cm^3. In δ-doping literature (b) it is more common to describe the profile by its Gaussian FWHM, with the depth referring to the distance from the surface to the center of the Gaussian profile. (*Adapted from (a) Papasouliotis*[128] *and (b) Gossmann*[129])

4.1.3 How is shallow doping achieved?

Considered broadly, creating ultra-shallow doping profiles is composed of two challenges: how do you place the dopants in the host semiconductor, close to the interface? And having done so, how can you anneal the sample to render dopants electrically active without losing your shallow doping profile to diffusion? The latter is usually com-

plicated by the former, as implantation techniques result in damage to the host lattice which greatly enhances dopant diffusion[130]. Variations on conventional ion implantation such as cluster implantation[131] or plasma doping[128;132] essentially aim to reduce the implantation energy, which helps to achieve shallow dopant placement while minimising (but not eliminating) crystal damage. Developments in the annealing step seek to improve speed, having advanced through standard furnace annealing (minutes), rapid thermal processing (seconds)[133], flash-lamp annealing (milliseconds)[128] and pulsed laser annealing (milli- to nanoseconds)[132].

In recent years the demands on junction depth have become so severe that new approaches to shallow doping are required. Despite the remarkable progress in implantation technology, ultimately the crystal damage imposes a limit on achievable depths. As we shall see in a subsequent section, this limit appears to be 8 nm, which is insufficient for ITRS targets beyond 2013[1]. This has motivated work on **damage free**, surface mediated techniques. The monolayer doping technique from the Javey group[125] has demonstrated the potency of this approach, producing junction depths as shallow as 2 nm in silicon[134]. In this chapter we investigate the merits of the low-temperature δ-doping technique as a route to ultra-shallow doping.

4.1.4 How is shallow doping characterized?

While the fabrication of ultra-shallow doping profiles is challenging, there is a parallel and directly related challenge in reliable *metrology* of such structures. The development of a doping process relies on feedback from measurements of the physical dopant distribution and sheet resistance. In this chapter we will employ the *in situ* nanoprobe system to perform sheet resistance measurements, but an awareness of what other measurement techniques are used and what limitations they face will be useful. This discussion is not intended to be comprehensive, but covers the techniques we will refer to later in the chapter.

4.1.4.1 Physical characterization: Where are the dopants?

Secondary ion mass spectroscopy (SIMS) is a widely used technique for physical depth profiling in semiconductors - for a detailed review of the technique see Schroder[86]. The principle of the technique is to sputter material from the surface of the sample and analyze the small fraction of ionized species (secondary ions) in a mass spectrometer. The mass selectivity and dynamic range are excellent, with detection limits down to concentrations of 10^{14}cm^3. To obtain a depth profile the ion signal is recorded as a function of the sputtering time - the former is mapped to a concentration with the aid of a reference sample while the latter is mapped to a depth by knowledge of the sputtering rate. Example profiles are shown in Figure 4.1.

For ultra-shallow junction metrology the primary challenge of SIMS is in reducing the

sputtering energy, for two reasons. High energy species penetrate deeper into the sample, with the result that the ejected species can originate from the top *few* layers of the sample instead of from the surface alone. This leads to broadening of the depth profile. In addition, high energy sputtering ions lead to an effect termed *ion mixing* whereby some collisions push target atoms deeper into the substrate instead of ejecting them. This leads to a well-known problem of overestimating the trailing edge of abrupt doping profiles, demonstrated in Figure 4.2. Here SIMS profiles of B:Si δ-doped layers appear progressively sharper as the sputtering energy is reduced.

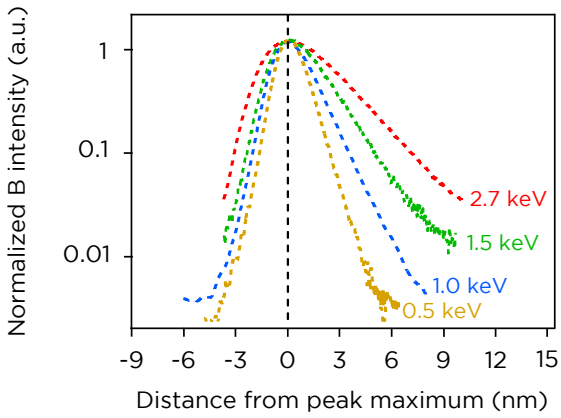


Figure 4.2: **Trailing edge artifact in SIMS characterization** Due to ion mixing effects, the trailing edge of SIMS profiles for δ-doped structures (here boron in silicon) are overestimated in proportion to the sputtering energy. (*Adapted from Baboux et al.*[135]).

Atom probe tomography (APT) is an emerging technique capable of resolving these sputtering-related issues with SIMS. Broadly speaking APT (see[136] for a review) is similar to SIMS in that atomic species from a sample are controllably ejected and analyzed. Uniquely, the analysis of ejected species is fully spatially resolved, allowing the profiling of materials in three dimensions with better than 0.2 nm resolution. If operated in a mode where the spatial data is integrated, 1D depth profiles like those from SIMS can be obtained. However the second unique feature of APT is the nature of material removal from the sample. Rather than sputtering, samples are prepared as thin needles and subjected to pulses of high electric fields. This controllably ejects atoms from the surface - as few as one atom per pulse. With no sputtering, APT is better suited than SIMS for measuring highly abrupt, narrow doping profiles as we will directly see in a later section.

4.1.4.2 Electrical characterization: How well are the dopants conducting?

In addition to the four point probe method (which by now the reader will presumably be quite knowledgeable about) there are two other electrical characterization techniques we will highlight, each useful for different reasons.

Spreading resistance profiling (SRP) is essentially depth profiling of *resistivity* rather than doping density. We saw in the previous chapter that for sufficiently small probe radii, spreading resistance dominates a 2-point probe measurement, and that this resistance can be expressed in terms of the probe radii and the material resistivity. SRP capitalizes on this by stepping two probes along a beveled sample edge to map out resistivity as a function of depth. The role of a bevel is to provide depth resolution (for example a 1 degree bevel angle with steps of 5μm would provide a depth resolution of 0.87 nm); but as a consequence the measurement is destructive and requires special sample preparation. The resulting spreading resistance versus depth curves are mapped back to either a free carrier density or a resistivity by comparison with a reference measurement on samples with well known doping profiles. Many correction factors are also necessary to account for the nature of the contacts and the sample structure; details of these as well as more general information about SRP can be found in Schroder[86].

The **junction photovoltage** (JPV) technique is a non-contact optical method of obtaining the sheet resistance and junction leakage of a p-n junction[137], which in the present discussion would be a shallow doping layer formed on an oppositely doped substrate. Carriers are photoexcited in the upper doping layer with a chopped light source, and diffuse through the layer until eventually recombining with carriers from the lower doping layer. This produces a surface photovoltage which can be measured with a non-contact surface Kelvin probe. By measuring the surface photovoltage as a function of the chopping frequency and comparing with a reference sample, the sheet resistance as well as the junction conductance and capacitance can be obtained. The technique fundamentally requires a p-n junction structure, but being fast and non-contact is an important advantage for reliably mapping sheet resistances in ultra-shallow junctions[134].

	Gives:	**Requires:**
SRP	• $n_D(d)$	• Bevelled sample edge • Reference sample for calibration
4PP	• R_S	• $\rho_{top} << \rho_{bottom}$
JPV	• R_S • Junction leakage	• p-n junction • Reference sample for calibration

Figure 4.3: **The three most common approaches to characterizing the electrical properties of ultra-shallow doping profiles** A table of three different experimental techniques commonly employed in ultra-shallow doping metrology, summarizing the output and applicability of each.

4.2 Thermal redistribution processes: how 'δ' is a δ-layer?

The goal of this chapter is to study how the low temperature δ-doping technique can be used to extend shallow doping to depths of only a few monolayers. When preparing and measuring samples at this scale it is essential that we possess a detailed understanding of how 'wide' a δ-layer really is. In this section we will examine thermal redistribution processes affecting the δ-layer samples we will grow, and what can be said about the true physical widths based on existing literature and our own depth profiling measurements.

Whenever we talk of a system being two-dimensional, it is always implied that we mean '2D relative to some important length scale'. In the previous chapter we demonstrated that the δ-layers we measured were 2D *relative to the probe separation* of $>50\mu$m. In this chapter we will investigate the resistivity of these layers as a function of encapsulation depth, and there is a new important length scale - we now must consider whether these layers are 2D *relative to their distance from the interface* of a few atomic planes.

It is true that the initial doping process is confined to a single atomic plane, but by the time the layer has been encapsulated, two thermally activated redistribution effects will have occurred, schematically depicted in Figure 4.4. These are **diffusion**, leading to symmetrical Gaussian broadening, and **segregation**, leading to an exponential decay towards the surface. In the following sections we will discuss the details of these processes, with the aim of determining how best to describe our δ-doping distributions on an atomic scale.

4.2.0.3 Diffusion

Possessing $\approx$ a quarter of a monolayer of impurities within a single atomic plane represents a very highly *ordered* system when considered in the vertical direction. Given sufficient energy to move, dopants will be driven by entropy to diffuse away from the original doping plane. This process can be quantitatively described by Fick's law, which relates diffusion to a concentration gradient. For a fixed number of dopants N_0 originally located in a sheet at a depth of $z = 0$, the doping profile after some time t is:

$$N(z,t) = \frac{N_0}{2\sqrt{\pi Dt}} exp\left(-\frac{z^2}{4Dt}\right)$$

with D the diffusivity coefficient. There are several approaches to determining D, but in cases such as ours where the doping density N_d far exceeds the silicon intrinsic carrier

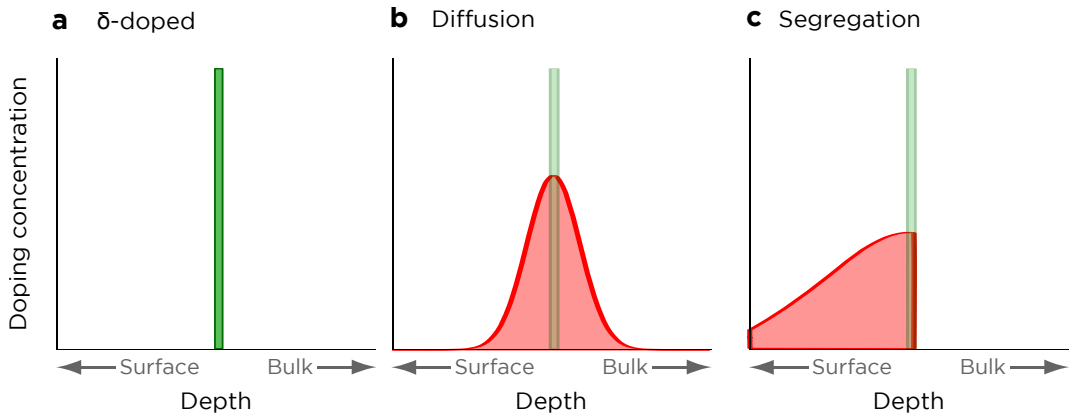


Figure 4.4: **Thermal redistribution processes for a δ-doping layer** While the initial doping profile is confined to a single atomic plane and resembles a true δ-doping profile (a), at finite temperatures dopants will redistribute. Elevated temperatures will cause symmetrical broadening through diffusion (b), while the encapsulation stage will induce segregation of dopants towards to the growth front (c).

concentration $N_i (\approx 1\times10^{15}$ cm^{-3} at 250°C), an *extrinsic* diffusion model is appropriate:

$$D(T) = 2\left[D_0^1 e^{E_A^1/kT} + D_0^2 e^{E_A^2/kT}\frac{N_d}{N_i} + D_0^3 e^{E_A^3/kT}\left(\frac{N_d}{N_i}\right)^2\right]$$

where the D^n and E_A^n are empirically determined coefficients particular to the choice of dopant and substrate. In the case of phosphorus in silicon, these values are known and well agreed upon in the literature[129]. An absolute upper limit for N_d (the equivalent 3D density of the delta-layer) can be obtained as:

$$N_d = (\sqrt{N_s})^3$$

yielding a value of 3×10^{21}cm^{-3} from a sheet density of 2×10^{14}cm^{-2}.

The two thermal processes we should consider are the incorporation anneal (350°C for 60 seconds) and the encapsulation stage (250°C for $\approx$ 20 minutes). For these temperatures and times, using the extrinsic diffusion model we would expect a strict δ-profile to broaden into a Gaussian of FWHM $\approx 3\times10^{-3}$nm (incorporation) and $\approx 9\times10^{-5}$nm (encapsulation)[†]. For perspective, the diameter of an atom is $\approx$0.1 nm; we can hence safely consider diffusion to be negligible at these low temperatures.

4.2.0.4 Segregation

The second redistribution process we must consider is that of dopant *segregation*, by which we mean the migration of dopants towards the surface during the encapsulation stage. We can describe this process with a simple model based on an incorporation prob-

[†]The script used to perform these calculations is given in Appendix B

ability, p. We assume that dopants on the surface are mobile, and with each new layer deposited some fraction (1-p) of these dopants migrate to the new layer (Figure 4.5). This results in an exponential decay in concentration towards the surface, with the $1/e$ decay length termed the *segregation length* Δ.

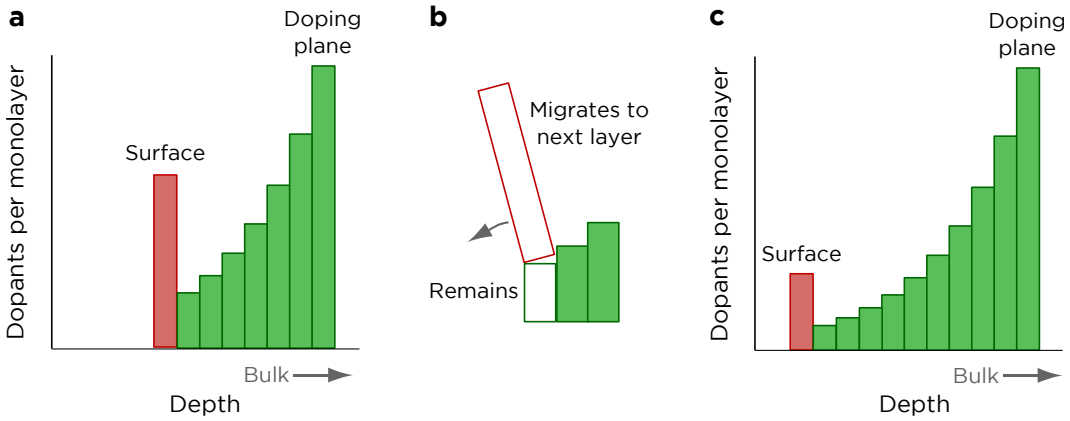


Figure 4.5: **The segregation of dopants during encapsulation** The simple incorporation probability model assumes that with each additional monolayer of encapsulation, some fraction (1-p) of the dopants will migrate to the surface of the new layer (b). Over the course of an encapsulation growth, this results in an exponential decay of dopants towards the growth front (c).

Assuming the monolayer thickness of the grown material is known, the resulting spatial distribution of dopants can then be described by knowing the single parameter Δ. However predicting this parameter is not trivial. Experimental studies of dopant segregation have demonstrated dependencies of Δ on the growth temperature[138;139], growth rate[140], dopant concentration[141] and material system[140], while theoretical models have predicted additional dependence on the surface vicinality[140;142]. To date there is no universal model which fully describes segregation. As a consequence, not only is it difficult to predict in advance what value of Δ to expect, it is also difficult to compare data sets across different experimental works.

Nonetheless, on the basis of the existing body of literature we may make *qualitative* statements about segregation. The two main control variables at our disposal are the growth temperature and growth rate. In order to minimize the segregation length we should maintain low growth temperatures ($\Delta \propto exp(T)$) and high growth rates ($\Delta \propto \sqrt{\frac{1}{R}}$). In practice a tradeoff must be made between low segregation lengths (requiring low temperatures during growth) and crystal quality/dopant activation (requiring high temperatures). Previous work on the Si:P system has indicated that a growth temperature of 250°C represents the ideal compromise[106;107]. Oberbeck *et al* studied the segregation length in Si:P systems under these growth conditions and with a growth rate of 0.27 nm/min[107] (comparable to the rates we have used in this thesis), using both SIMS and STM. From fitting to the leading edge of SIMS profiles they obtained a segrega-

tion length of 2.3 nm, whilst from STM experiments (in which the number of phosphorus atoms on the surface was counted before and after growing 5 ML of silicon) they obtained a segregation length of only (0.6±0.1) nm. They concluded that lower value of segregation length was correct, with the SIMS value distorted by broadening of the profile from the sputtering process.

4.2.0.5 Experimental tests of dopant redistribution

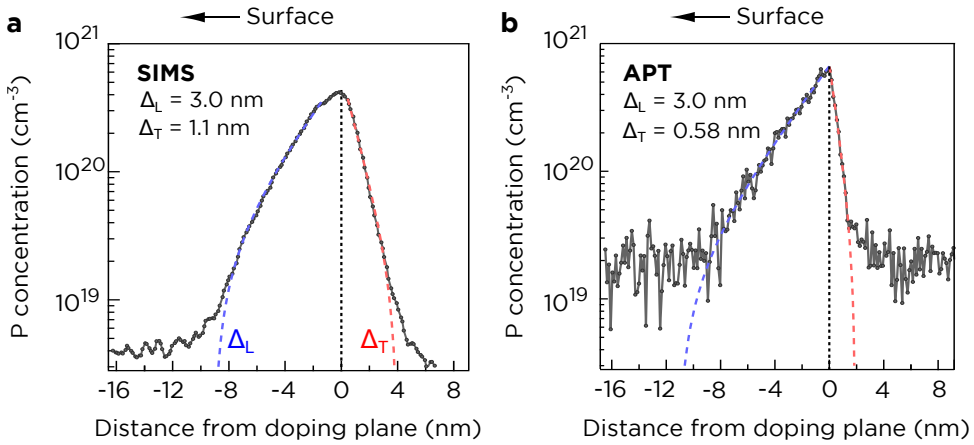


Figure 4.6: **Depth profiling of the physical dopant distribution by SIMS and APT** Physical dopant profiling techniques such as SIMS (a) and APT (b) offer a direct insight into the segregation and diffusion behaviour in δ-doping layers. Here both techniques agree on a segregation length Δ_L of 3 nm, while the diffusion length Δ_T is overestimated for the SIMS technique. These profiles confirm the discussion in the text regarding the relative importance of segregation and diffusion for these Si:P δ-layers.

The preceding discussions about diffusion and segregation capture the essential properties, but in reality both processes are enormously complicated. To reach a firm conclusion about the true width of our δ-doping layers it is thus important to obtain depth profiling measurements. In Figure 4.6 we show SIMS (a) and APT (b) profiles of Si:P δ-layer samples encapsulated with the typical conditions used in this thesis (250°C, ≈2 Å/min). The leading edge of these traces corresponds to segregation, and fitting an exponential to it gives a segregation length Δ_L of 3.0 nm in both cases. Since the two different methods agree and in particular the APT technique does not involve sputtering, we believe this value to be an accurate measure of the segregation in our particular samples.

The trailing edge of the profiles corresponds to diffusion of dopants into the substrate. As was previously discussed, SIMS measurements cannot accurately capture the trailing edge corresponding to diffusion. Fitting to the APT data gives a Δ_T of 0.58 nm, equivalent to a FWHM of 0.68 nm. This is two orders of magnitude higher than our estimate based on the extrinsic diffusion model (≈3 pm from section 4.2.0.3), but it is not clear whether this constitutes the true diffusion length or an instrumentation limit.

Regardless, it is obvious that segregation is the dominant redistribution process. In the coming sections we will see that this segregation is extremely important for describing the electrical behaviour of near-surface δ-doping layers.

4.3 Depth dependent four-probe measurements of Si:P δ-layers

In the previous two sections we dealt with the context and theory of near-surface δ-doping profiles. We now progress to describing the main experimental work of this chapter, which is the electrical characterization of δ-layers with encapsulation depths ranging from 0 nm to 20 nm. We will see that such measurements indicate a dramatic, reproducible transition between bulk- and surface-sensitivity at a depth of only half a nanometer ($\approx$4 monolayers). Beyond this depth the resistivity of the 2D layer decreases sharply, eventually saturating at depths beyond $\approx$20 nm.

4.3.1 The ultimate ultra-shallow junction

The logical starting point for our measurements is the *incorporated surface*. As discussed in the previous two chapters, this is a 2$\times$1 Si(100) surface which has been saturation dosed with PH_3 and then annealed to incorporate phosphorus atoms into the top layer of the silicon lattice. This is an interesting configuration in that it represents the theoretical endpoint of ultra-shallow junction scaling: an extremely high density of dopants confined to a single atomic plane at a depth of precisely zero nanometers from the surface.

A previous scanning tunneling spectroscopy study by Reusch *et al* indicated that the incorporated surface is semiconducting[143], suggesting that some amount of encapsulation of the dopants in silicon is required to create the familiar metallic 2D conduction. In Figure 4.7 we show four-terminal resistance measurements on two different substrate types, before and after dosing and incorporating. The measurement technique was discussed at length in the previous chapter. As we saw in that chapter, p-type substrates yield a $\frac{1}{s}$ probe spacing dependence which reflects transport through the bulk substrate, while n-type substrates exhibit larger resistances which are scattered but overall independent of the probe spacing. This is a consequence of a surface inversion layer for n-type samples, discussed previously. Importantly, we cannot observe any real difference in the measurements between the clean and incorporated samples. This indicates that the layer of dopants at the surface are not electrically active, in agreement with the findings of Reusch.

We then have an answer regarding the 'ultimate' ultra-shallow junction - at this extreme endpoint, the doping profile is no longer useful as an electrical device. This ob-

servation nicely frames the results which follow - since we know the surface is semiconducting at 0 nm but metallic at ≈4 nm, what is the nature of the transition between these depths?

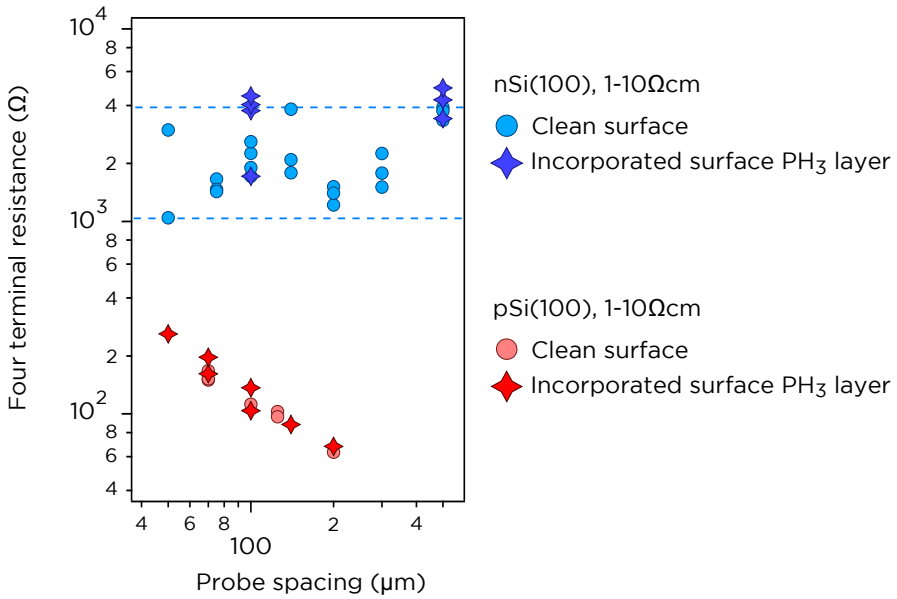


Figure 4.7: **Four-terminal resistance measurements of 'zero depth' δ-layer samples** Measurements of Si(100) samples made before (circles) and after (stars) dosing with PH_3 and incorporating. For both p-type (red) and n-type (blue) substrates the phosphine does not alter the measurement results, indicating that a 'zero depth' δ-layer is not conductive.

4.3.2 Depth dependence of the δ-doping layer resistivity

4.3.2.1 Experimental method

In chapter 3 we outlined the method for creating Si:P δ-doping profiles with an epitaxial encapsulation layer ≈4 nm thick. The process we will follow in this chapter is mostly identical, except we will perform repeated cycles of silicon overgrowth and 4PP measurements. In this way within any given data set we are following the evolution of a single sample. The silicon flux from the sublimation cell is slow (≈2 Å/min) and stable, such that thickness steps of 5 Å are readily achievable. We have until now been stating approximate growth rates from the sublimation cell, but for experiments where we assign particular significance to the encapsulation depth, it is critical that the growth rate be accurately and precisely known. It is hence worth briefly discussing the two methods used to obtain growth rate calibrations.

When beginning a new experiment, we must assume a growth rate based on experiments in the recent past. At the completion of the experiment, each sample is overgrown with a thick encapsulation layer (>30 nm). The clamps of the sample holder act as a mask for this growth step, such that when the sample is removed a step can be observed where

the sample was clamped (Figure 4.8). Careful measurement of this step with a stylus profilometer or atomic force microscope (AFM) gives an accurate step height. Combined with the known total growth time, this yields the growth rate with a typical uncertainty of better than 5%, which can then be used to correct the thicknesses in the preceding experiment. Independent confirmation of this calibration can be obtained by SIMS or APT profiling, which reduces the uncertainty to below 1% and agrees with step-height calibrations.

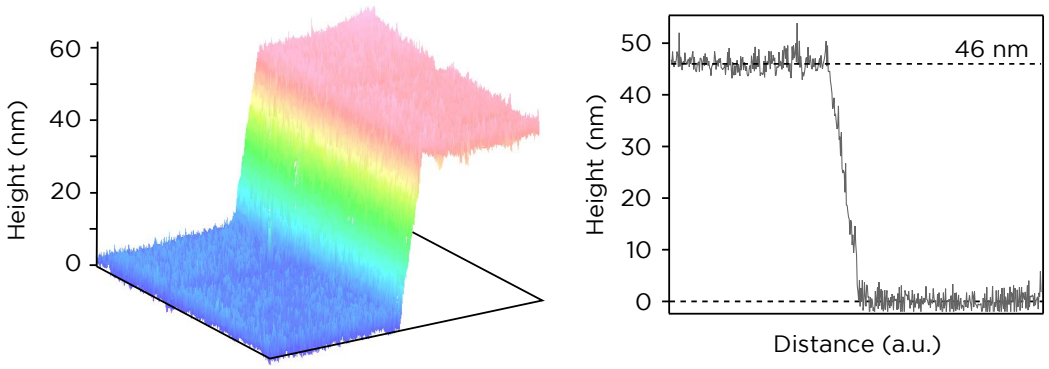


Figure 4.8: **Routine calibration of the silicon growth rate.** The clamps holding the sample in place serve the additional purpose of masking a section of the sample from silicon growth. By growing thick layers and measuring the step height with AFM (shown) or stylus profilometry, the growth rate can be determined on a sample-by-sample basis.

4.3.2.2 Depth-dependent electrical characterization results

As we found in chapter 3, it is helpful to begin by examining single probe tip-sample I-V characteristics. This involves holding the sample at ground potential and applying a ramped DC bias to one of the measurement probes while recording the current flow. Plotted as $\ln(\frac{dI}{dV})$, we saw in chapter 3 that such measurements provide qualitative information about the nature of the sample and probe contact. In Figure 4.9 we show such a plot as a function of encapsulation depth, in this case on a 100Ωcm p-type substrate. At the two extremes of depth in this plot we see traces that match our findings in chapter 3. On the incorporated surface (0 nm) the contact is strongly rectifying, with limiting shunt and series resistances at high and low biases respectively. At an encapsulation depth of 4.1 nm, the rectification has been eliminated and the conductance is an order of magnitude higher. The interesting aspect of Figure 4.9 is the transition between these two extremes. The rectification is abruptly eliminated after only 0.5 nm of encapsulation, which for perspective is less than four monolayers of silicon (1 ML = 0.136 nm). As the layer is buried deeper, the conductance steadily increases.

These trends in the tip-sample conductance are matched by four-probe resistance measurements. In Figure 4.10 we show probe-spacing dependent resistance measure-

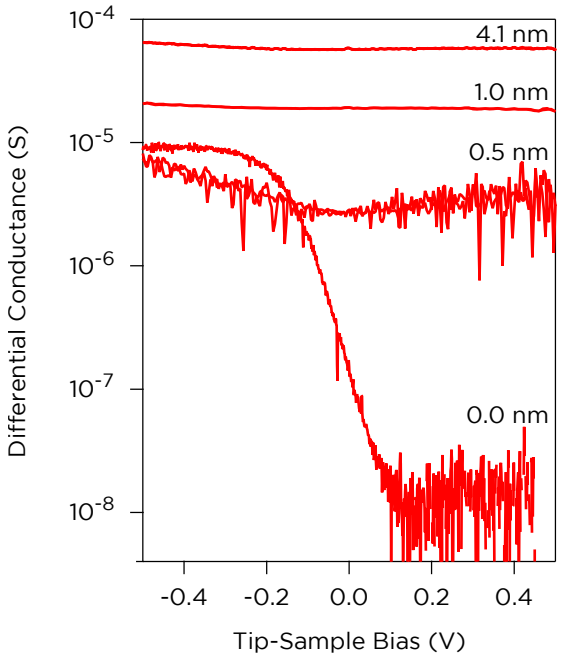


Figure 4.9: **Tip-sample conductance as a function of encapsulation depth.** The current-voltage characteristics reflect the changes in the sample conductivity as the δ-doping plane is encapsulated with epitaxial silicon. The abrupt elimination of rectification between 0.0 and 0.5 nm suggests electrical activation of the dopant layer.

ments as a function of encapsulation depth, this time using a 7 Ωcm p-Si(100) substrate. Recall that measurements made as a function of probe spacing can be used to discriminate between 3D (bulk) and 2D (δ-layer) conduction. In Figure 4.10 we see a transition from bulk conduction (R$\propto \frac{1}{s}$) at 0 nm to δ-layer conduction (R=constant) at 1.8 nm, followed by a steady decrease in resistance as the encapsulation depth is increased.

The trends seen in Figures 4.9 and 4.10 are reproducible. In Figure 4.11 we plot the results of 6 different samples, using both p- and n-type substrates with resistivities varying from 7 to 100 Ωcm. We see that initially (<5 nm) the four-probe resistance decreases sharply with increasing encapsulation, eventually saturating at depths in excess of 20 nm. Note than in this and all subsequent Figures, we show only measurements which have a 2D rather than 3D signature. Error boxes are included in Figure 4.11, though for many of these datapoints the error is not visible on this scale. The depth uncertainty arises from the uncertainty in growth rate, and as such should be interpreted as a systematic error - i.e. all datapoints will move together if the growth rate changes. The vertical error corresponds to the variation observed from measurements at several different probe-spacings and locations on the sample.

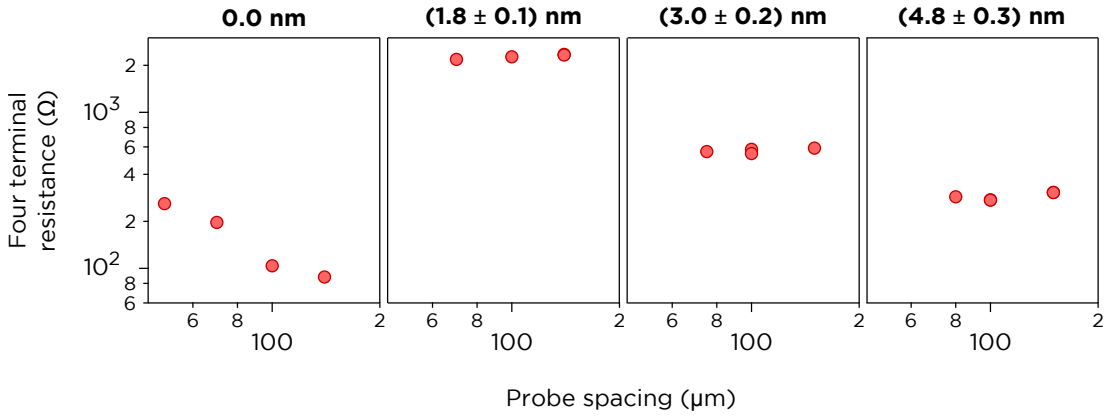


Figure 4.10: **Probe spacing dependent resistance measurements of δ-doped silicon as a function of encapsulation depth.** An abrupt transition between 3D (R$\propto \frac{1}{s}$) and 2D (R=constant) conduction is seen between encapsulation depths of 0 and 1.8 nm, after which the 2D resistance steadily decreases. This is consistent with the δ-doping layer becoming electrically active and then progressively more conductive.

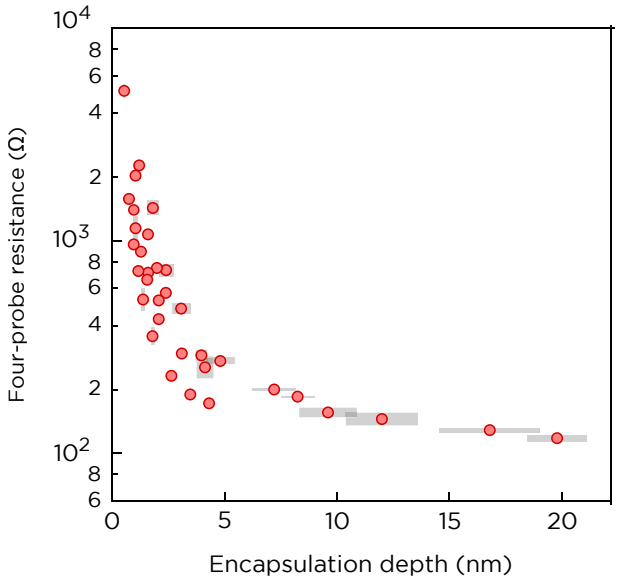


Figure 4.11: **A compilation of the depth-dependent four-probe resistance of Si:P δ-layers at room temperature** A combined plot of data sets from 6 different Si:P δ-layer samples as a function of the encapsulation depth. There is some variation between samples, but the qualitative trend is common to all data sets. Grey boxes indicate uncertainties.

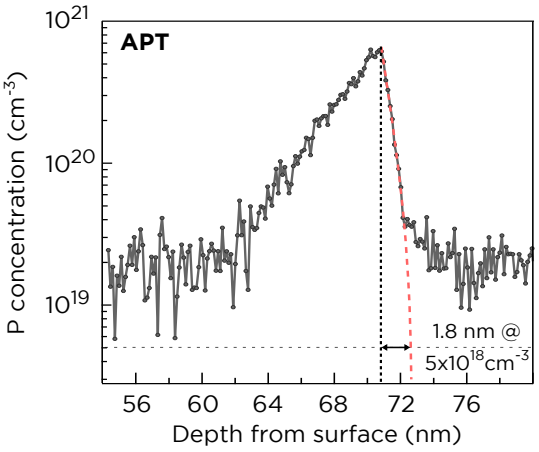


Figure 4.12: **Defining the junction depth of a δ-layer** For an equitable comparison to existing ultra-shallow junction literature, we must determine the depth at which the trailing edge of the doping concentration profile falls to 5×10^{18}cm^{-3}. As discussed previously, the APT technique is the most suitable means of measuring the trailing edge of a δ-layer. Doing so in this figure gives a width of 1.8 nm, for a junction depth of ≈72.5 nm.

4.3.3 Depth dependence in context

In the following section we will be concerned with a physical model for this trend, and attempt to explain both the decreasing resistivity as well as the abrupt 'turn on' at ≈5Å. Before this undertaking however, it is instructive to provide some context for the results in Figure 4.11 to demonstrate their significance. Since we are confident that this data corresponds to conduction through a 2D layer we can reliably map the resistances to sheet resistivities, which then enables a comparison with literature results for state-of-the-art ultra-shallow junctions.

As discussed earlier there are several approaches to defining junction depth, so for a fair comparison it is important that we use a consistent definition. The most common is 'the depth from the surface at which the doping density has reduced to 5×10^{18}cm^{-3}'. In Figure 4.12 we show an atom-probe tomography profile for a δ-doped layer, this time extrapolating the trailing edge to obtain the width at a phosphorus density of 5×10^{18}cm^{-3}. A value of 1.8 nm is obtained; this is much larger than our diffusion estimate in section 4.2.0.3 and may be an instrumentation-limited overestimate, but we can at least treat this as a definitive upper bound. Since we showed in section 4.2.0.3 that this diffusion length is essentially entirely determined by the incorporation anneal as opposed to accumulating over the encapsulation period, we may hence define our junction depth as the encapsulation thickness plus a constant 1.8 nm.

In Figure 4.13 we plot a depth dependent data set (one for which we have SIMS profiling for maximum confidence in the depth calibration) together with a compilation of previously reported room temperature sheet resistances for both ion-implantation[128;131;132;133;144;145;146;147]

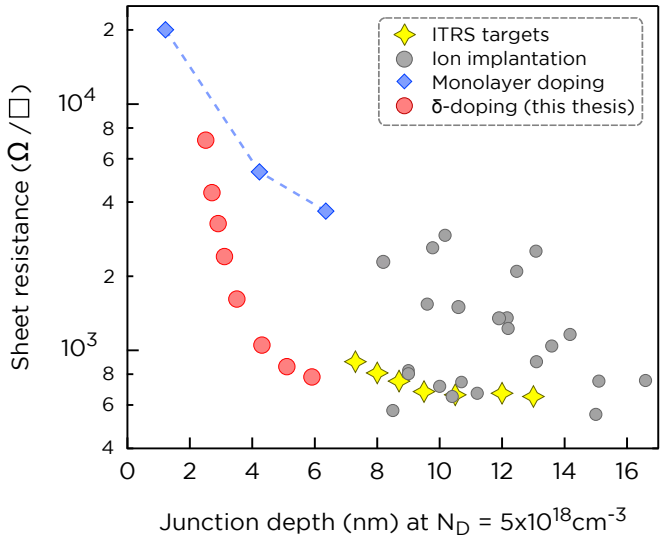


Figure 4.13: **A comparison of near-surface Si:P δ-layers with existing ultra-shallow junctions.** When compared to the 2011 - 2015 ITRS targets (yellow stars,[1]) for junction depth and resistivity, the Si:P δ-doping method studied in this thesis (red circles) can be seen to be extremely promising. The achievable depths far surpass those of implantation techniques (grey circles,[128;131;132;133;144;145;146;147]), and much lower resistances can be achieved compared to the monolayer doping technique (blue diamonds,[134]). Here the depth on the x-axis refers to the distance from the surface at which the doping density falls below 5×10^{18}cm^{-3}.

and the surface-mediated monolayer doping technique from the Javey group at Berkeley[134]. We also include the ultra-shallow junction targets from the ITRS semiconductor scaling roadmap for 2011 though 2015[1]. The importance of our δ-layer results becomes immediately apparent. We see that with this gaseous phase doping and low temperature silicon encapsulation we obtain doping profiles which surpass not only all projected ITRS requirements but also all reported literature results to date. Importantly it is worth remembering that we are using a conservative upper bound for the diffusion length, which suggests that the results we present here are likely to be even more impressive than Figure 4.13 suggests.

It is interesting to consider what physical effects are driving the increase in resistivity at shallow depths. This may provide insight into both the limitations facing all ultra-shallow junctions as well as indicate avenues to optimize our Si:P δ-layer resistivities. Such an investigation is the subject of section 4.4.

4.3.4 How *electrically* wide is a delta layer?

For all of this discussion about achieving shallow doping profiles, we should not forget that ultimately it is not the distribution of *dopants*, but *free carriers* which matters, as the latter is what determines electrical characteristics. If the goal is to obtain shallow *electrical*

profiles, shallow *doping profiles* are necessary but not sufficient. The relationship between a doping profile and the resulting free carrier distribution is classically described in terms of the Debye length, but if the dopant distribution becomes smaller than the free carrier de Broglie wavelength a new, quantum mechanical relationship applies. Below we will briefly describe these two limits, followed by a discussion of what can be said about the carrier distribution in our δ-layer samples.

Classical charge distributions (wide doping profiles)

Previously we discussed the diffusion of dopant atoms driven by a concentration gradient. The same effect results in a redistribution of free electrons (or holes, but for clarity we will henceforth assume electron majority carriers). Abrupt changes in doping density cause electrons to diffuse (or 'spill') into regions of lower doping density. This creates a charge separation, and the resulting electric field causes electrons to drift back. An equilibrium between these processes is reached, with the final charge distribution described by the Poisson equation, with a characteristic length scale of the **Debye length**:

$$L_D = \sqrt{\frac{\epsilon kT}{e^2 n}} \tag{4.1}$$

where ϵ is the material permittivity, e the elementary charge and n the carrier density. The Debye length is also called a screening length; the connection to screening here is that charge is rearranging (drifting) to screen the electric field established by carrier diffusion.

Given that we are discussing a dopant junction, which of the carrier densities in Equation 4.1 applies? Both sides of the junction will possess their own Debye length, but in asymmetric (i.e. N+/p) junctions it is the lower doped side which dictates the depletion width. This is illustrated in Figure 4.14a, where we have obtained the carrier distribution for two different ultra-shallow doping junctions using a 1D Poisson solver[99]. The heavily doped N-type layer is 5 nm wide at a concentration of 1×10^{20}cm^{-3} in both cases, but the substrate doping is reduced from 5×10^{18}cm^{-3} in the upper plot to 1×10^{15}cm^{-3} in the lower. It is clear from the depth scales that the 'electrical' depth of the N-type layer is different in these two cases, with much less redistribution for the heavier doped substrate. This is the reason for substrate doping being a 'scaled' parameter in the microelectronics industry; the current standard substrate doping level is 5×10^{18}cm^{-3} for the express purpose of obtaining short Debye lengths and hence electrical widths.

Quantum mechanical charge distributions (narrow doping profiles)

The preceding discussion about Debye screening lengths does not apply when we turn to degenerate, highly confined doping layers. The reason for this is the quantization of energy levels which is characteristic of a 2D system (Figure 4.14b). Carriers are no longer able to redistribute continuously, because only particular energy levels are permitted. Instead of solving the Poisson equation to describe the charge distribution, we

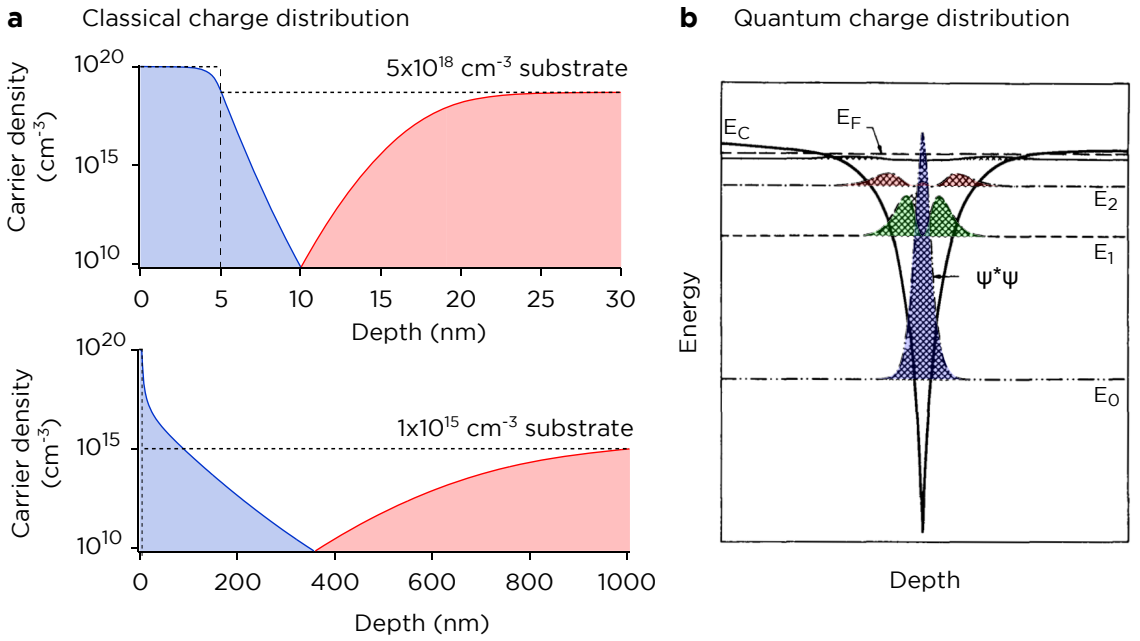


Figure 4.14: **Describing the free carrier distribution of doping profile in the classical and quantum regimes** In the absence of quantization effects, the distribution of free carriers in a dopant junction is dictated by the Debye length of the lower doped side of the junction (a). A surface 1×10^{20}cm^{-3} doping layer which is physically 5 nm deep becomes only a few nanometers deeper electrically when on a 5×10^{18}cm^{-3} substrate (upper plot), but is hundreds of nanometers wider when formed on a 1×10^{15}cm^{-3} substrate (lower plot). In contrast, if the impurity profile is narrow compared to the carrier de Broglie wavelength, the distribution of free carriers must satisfy the Schrödinger equation and is quantized into different subbands (b).*(Poisson calculations (a) performed with the Snider package[99], band structure (b) adapted from Gossman[129])*

now must self-consistently solve the Poisson and Schrödinger equation. The Poisson equation describes how electric fields are arranged for a given charge distribution, while the Schrödinger equation describes what charge distributions are possible given the arrangement of electric fields. The resulting charge distribution is now described by the quantum mechanical wavefunctions of the occupied subbands, as schematically shown in Figure 4.14b. For δ-doped silicon this quantization can be experimentally observed at room temperature in capacitance-voltage profiles[129;148] and at low temperatures in carrier mobility measurements[149] and resonant tunneling experiments[149]. In the context of quantum-confined δ-layers, the charge distribution is usually described in terms of the FWHM of the carrier distribution, which provides the distance over which 76% of the carriers are located.

Based on the preceding discussion, what can we say about the electrical width of our shallow δ-doped layers? The quantum and classical descriptions merge smoothly as the impurity distribution becomes shallower or wider[149] and the subband energy spacing re-

duces to zero. The Si:P δ-layers measured in this thesis have been the subject of extensive theoretical study in the deep limit (i.e. far from the interface)[120;150;151;152;153]. These studies indicate that carriers will be strongly confined, even at room temperature. However we note that the band structure will be strongly perturbed at very shallow encapsulation depths, as the silicon-vacuum interface represents an infinite potential step and will alter the solutions to the Schrödinger equation. In the absence of bandstructure calculations for the specific sample geometries studied here, it is difficult to predict whether we should expect a quantum mechanical carrier distribution. A full investigation is beyond the scope of this thesis, but forthcoming experimental studies of shallow Si:P δ-layers with angle resolved photoemission spectroscopy[154] and low temperature scanning tunneling spectroscopy[155] will be illuminating in this respect.

If quantum confinement is not considered and we were purely to determine the width based on the classical regime, the low substrate doping we are using would result in electrical widths of hundreds of nanometers (Figure 4.14a). Since we are using probe separations of tens of micrometers, this would still appear 2D in our measurements. But importantly, whether the carrier distribution is nanometers or hundreds of nanometers our main findings in this chapter are not significantly altered. If the substrate Debye length is indeed important, reducing the 'electrical width' of the δ-layers would simply be a matter of employing higher doped substrates, with no other changes to the fabrication process. While this might necessitate the adoption of a non-contact characterization method such as junction photovoltage, the information gleaned from our four-probe measurements on lower doped substrates would remain relevant.

4.4 Building a model for the depth dependent conductivity

We have now seen that the resistivity of a highly doped Si:P δ-layer is strongly dependent on how deeply it is buried, particular for the first 5 nm. In this section we advance a model to account for this trend based on the finite segregation length of the δ-layer combined with a simple surface scattering model. We will also discuss more complicated effects which could be taken into account to build a more complete model. Finally, we will also discuss the nature of the abrupt transition between bulk and surface sensitivity in the four-probe measurements.

At this stage it will be helpful to adjust how we are plotting the depth dependence data. It is the resistivity which we are interested in[‡] but any change in resistivity is reflect-

[‡]Recall from chapter 3 than we can map four-terminal resistance to sheet resistivity using a $\pi/ln2$ correction factor - provided we are sure that conduction is 2D

ing a change in one or both of the more fundamental quantities: mobility μ and carrier density N_S:

$$R_S = \frac{1}{q\mu N_S}$$

Since this is an inverse relationship, it will be more intuitive to instead plot the conductance ($1/R_S$), expressed in units of the conductance quantum G_0 ($= 2e^2/h$). Our task will then be to consider depth-dependent influences on the mobility and carrier density, increasing the complexity until we are able to adequately account for the experimental data.

4.4.1 A preliminary model: the role of segregation

In section 4.2.0.4 we discussed the segregation of dopants towards the surface during overgrowth. It follows that for encapsulation depths comparable to the segregation length, a non-negligible fraction of the dopants will reside on the surface. We have already seen in section 4.3.1 that these dopants are electrically inactive. A simple approach to determining the total number of active dopants as a function of encapsulation depth is to integrate over the monolayer density up to but excluding the surface (i.e. the green bars in Figure 4.5a and b). Using the incorporation probability model in section 4.3.1 then yields an active carrier density which has an exponential depth dependence:

$$N_s(d) = \int_0^d n_{tot}\left[1 - exp\left(\frac{-z}{\Delta}\right)\right].dz = n_{tot}(1 - e^{\frac{-d}{\Delta}}) \tag{4.2}$$

with d the encapsulation thickness, Δ the segregation length and n_{tot} the total number of dopants introduced at the δ-doping stage. In fact we can do even better than this by directly integrating the SIMS depth profile, which captures any deviation in the segregation profile from the idealised incorporation model. This method is depicted in Figure 4.15.

As a starting point if we make the assumption that the carrier mobility remains constant, the conductivity becomes:

$$\sigma(d) = q\mu n(d) = \sigma_\infty \frac{n_d}{n_\infty} \tag{4.3}$$

where $\frac{n_d}{n_\infty}$ is obtained from integrating the SIMS profile and σ_∞ is the limiting value of conductance for very deep encapsulations, which can be estimated from Figure 4.11. In Figure 4.16 we plot the prediction of this model together with data from a single experiment (7 Ωcm p-Si substrate). We have selected this data set for the discussion in this section since we have SIMS profiling data for this sample.

Two things are apparent in Figure 4.16 - the segregation-based model for the active carrier density captures a substantial degree of the observed depth dependence, but at the same time it is overestimating the conductivity. This tells us that while this simple

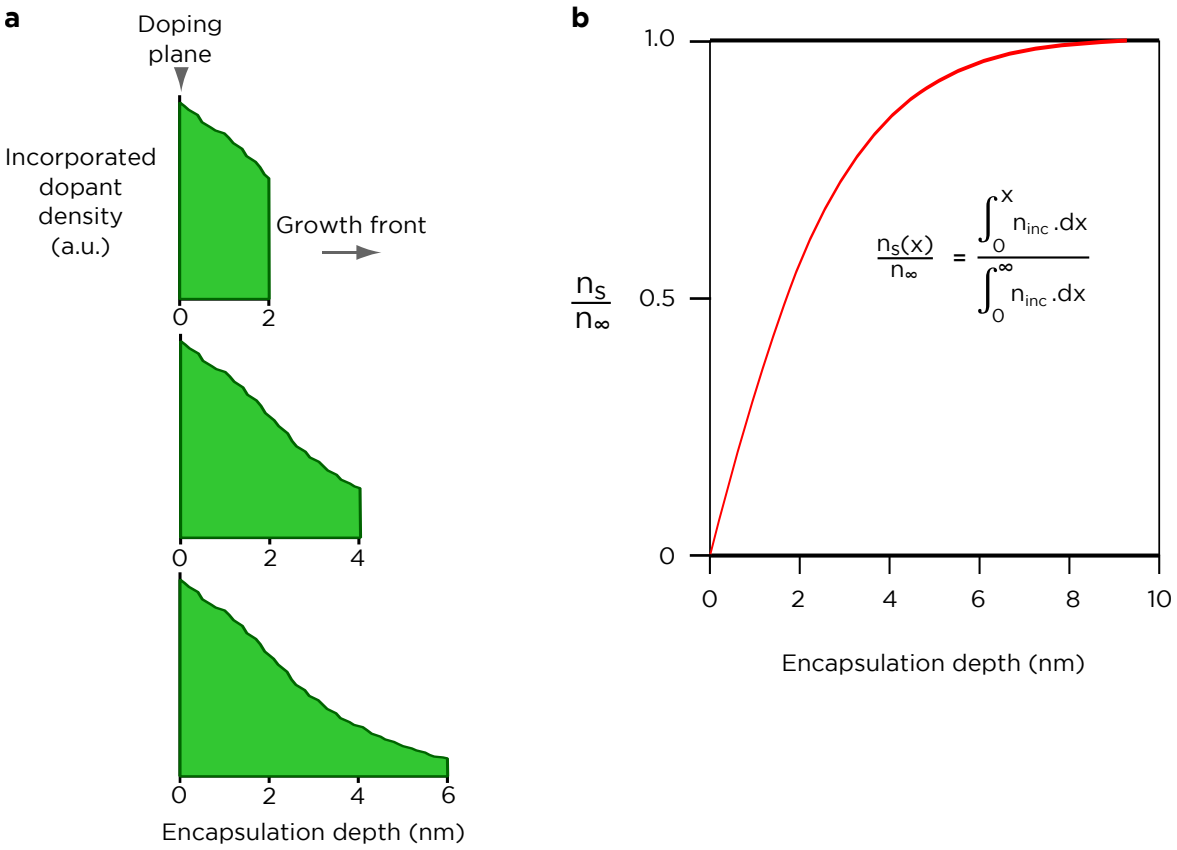


Figure 4.15: **The role of segregation in imposing a depth-dependent carrier density.** Given the assumption that dopants residing *on* the surface are not electrically active, the segregation tail can be integrated at each growth step (a) to produce a depth-dependent 'fraction of active dopants', shown in (b).

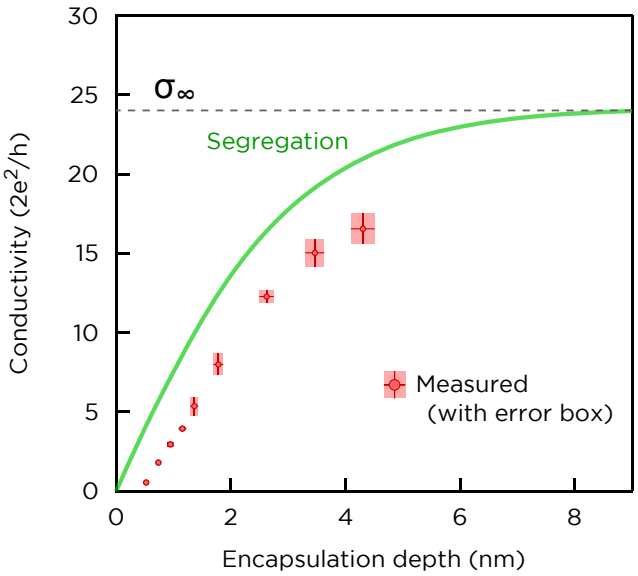


Figure 4.16: **A segregation-based constant mobility model for depth-dependent conductivity in a δ-doping layer.** By accounting for a finite segregation length, we are able to infer a depth-dependent conductivity which is qualitatively similar to the experimental measurements. The overestimation of the experimental conductivity indicates that additional corrections should also be considered.

model is good for a first approximation, something more is required to accurately account for the experimental data.

4.4.2 An improved model: the role of surface scattering

Intuitively, constant carrier mobility at all depths does not seem like a very reasonable assumption, and it is perhaps unsurprising that we overestimated the near-surface conductance. There are a variety of ways in which the carrier mobility may be affected close to the interface; we will attempt an overview shortly but for now we consider only the role of *surface scattering* using the Fuchs model.

Originally developed to describe the resistivity of thin metal films, the Fuchs model employs a scattering parameter p to describe the relative proportion of elastic (p) to inelastic ($1-p$) scattering events at the surface[156]. The value of p depends on such factors as the surface roughness potential, Coulomb potentials of adsorbates or surface electron-phonon interactions, and as such tends to be treated as a phenomenological factor. In the limit of large depths d relative to the electron mean free path λ the Fuchs expression reduces to[117]:

$$\frac{\rho}{\rho_\infty} = 1 + \frac{3}{8}\frac{\lambda}{d}(1-p) \tag{4.4}$$

Where ρ_∞ is the resistivity in the absence of any surface scattering. For the present

purposes it is preferable to restate the Fuchs expression in terms of a conductivity modification:

$$\frac{1}{\sigma(d)} = \frac{1}{\sigma_\infty}\left(1 + \frac{3\lambda(1-p)}{8}\frac{1}{d}\right) \tag{4.5}$$

$$\sigma(d) = \sigma_\infty / \left(1 + \frac{3\lambda(1-p)}{8}\frac{1}{d}\right) \tag{4.6}$$

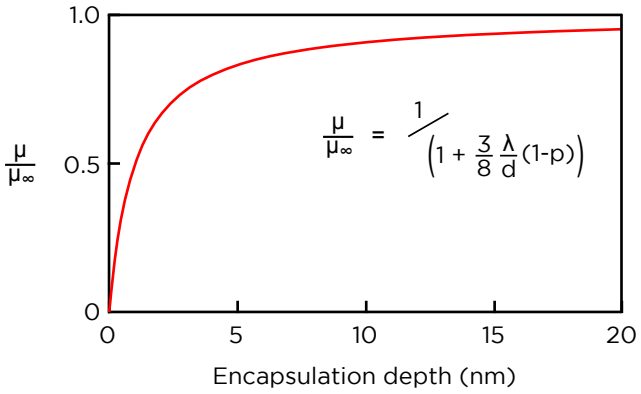


Figure 4.17: **An example of depth-dependent mobility from the Fuchs model for surface scattering.** Using example values of λ=5 nm and p=0.5, the mobility of a 2D film according to the Fuchs model is plotted.

In Figure 4.17 we plot the Fuchs correction (interpreted as a change in mobility) for example values of λ=5 nm and p=0.5. In trying to fit this model to the experimental data we encounter the difficulty that neither the mean free path nor the specularity parameter are precisely known for the samples discussed here. However we *are* able to place upper bounds on these values, such that we can simply leave them as fitting parameters and afterwards verify that they settle on realistic values. In Figure 4.18 we show the improvement made to the simple segregation model by including a Fuchs scattering term. The model now provides a much better description of the data, deviating only at depths below ≈2 nm. The fit shown corresponds to a value of 2.7 for the product $\lambda(1-p)$. Given that we expect mean free paths of ≈10 nm in these Si:P δ-layers[24;157], this corresponds to a specularity parameter p ≈0.75. Is this reasonable? In general the nature of the surface scattering depends on the ratio of the electron mean free path to the root-mean-squared roughness (h) of the surface, with primarily specular scattering when $h \ll \lambda$[117]. In Figure 4.19 we show representative STM images of a sample surface at various stages of encapsulation. In all cases we obtain an RMS roughness on the order of 0.1 nm, 100× less than the mean free path. Therefore we believe the values of λ and p obtained as fitting parameters in Figure 4.18 are plausible.

Some caution is required regarding the use of Fuchs' theory here. We have seen that by including it in our conductivity model with realistic parameters, we achieve good

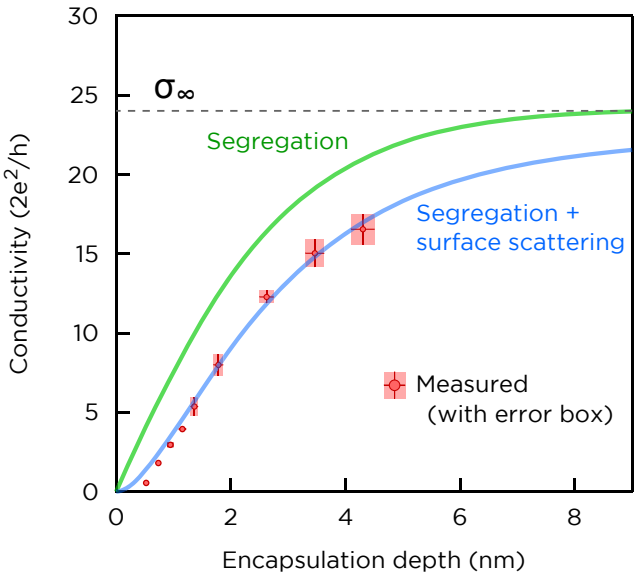
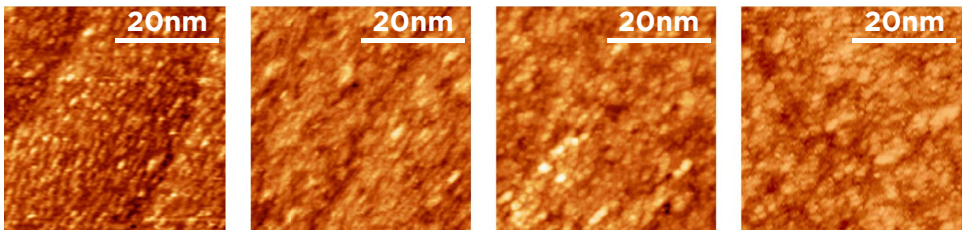


Figure 4.18: **A combined model for the depth-dependent conductivity of an Si:P δ layer.** By including a $1/d$ surface scattering term in the segregation model (green) we obtain a combined model (blue) which gives a much improved fit to the experimental data.



Encapsulation thickness (nm):	0.0	1.0	2.0	4.0
RMS roughness (nm):	0.11	0.10	0.11	0.13

Figure 4.19: **STM measurement of the surface roughness during encapsulation.** Representative STM images of the sample surface during encapsulation, for depths ranging from 0 to 4 nm. The RMS roughness of ≈0.1 nm remains substantially lower than the electron mean free path of ≈10 nm, suggesting that surface scattering will be primarily specular.

agreement with the experimental data. This observation is suggestive, *but not conclusive* evidence that the Fuchs model is appropriate for the data presented. In particular we have employed the simplest model of surface scattering, which does not account for quantized energy levels[116], angle dependent specularity[158] or atomic terrace step-edges. However at the same time it is desirable to formulate the simplest model possible - with the fewest free parameters - to avoid overfitting. In a following section we will review other effects which may influence the conductivity, and at the conclusion of this chapter we will suggest future experiments to provide the data required for a more complete physical model.

4.4.3 The minimum observed conductance

In examining depth dependent tip-sample I-V curves in Figure 4.9, we saw that the qualitative nature of the sample conduction appeared to change abruptly between 0 and 0.5 nm. This was confirmed in the depth and probe-spacing dependent resistance measurements in **??**, where a change from bulk to δ-layer conduction was seen between 0 and 1.8 nm. It is hence interesting to look at the lowest measurable depth (or equivalently conductivity) at which transport is 2D, and to consider whether there is any physical significance to this limit. Figure 4.20 plots the set of all conductivity measurements taken at a depth of less than 1.4 nm (note the horizontal scale, 1ML = 0.136 nm). This excludes any measurement where the conduction was found to be bulk-like (i.e. dependent on probe spacing) - the range over which bulk-like conduction was recorded is denoted by the shaded grey area.

What can we take from Figure 4.20? The shallowest measurements correspond to a depth of 4 monolayers, with conductivities at that depth of (0.52 - 0.55) G_0. Interestingly, this value is very close to the universal Ioffe-Regel criterion in 2D of 0.5 G_0 [159;160]. Conceptually this limit corresponds to the electron mean free path (λ) becoming comparable to the lattice spacing, and is the point of transition into a strong localization regime where the Drude conductivity model breaks down. However we should approach such an interpretation with caution, as the experimental data is not sufficient to conclusively show that a limit of 0.5 G_0 is not simply coincidental. We could also explain the transition in terms of the spreading resistance model outlined in chapter 3. At the shallow limit of the measurements in Figure 4.20 the 2D conductivity is dropping very rapidly, such that by $\approx$2 ML the 2D conduction path - if still present - would no longer dominate the substrate and thus would not be detected by four-probe resistance measurements. Temperature dependent resistance measurements would be helpful for further study, ideally to below the substrate freezeout temperature and as a function of encapsulation depth.

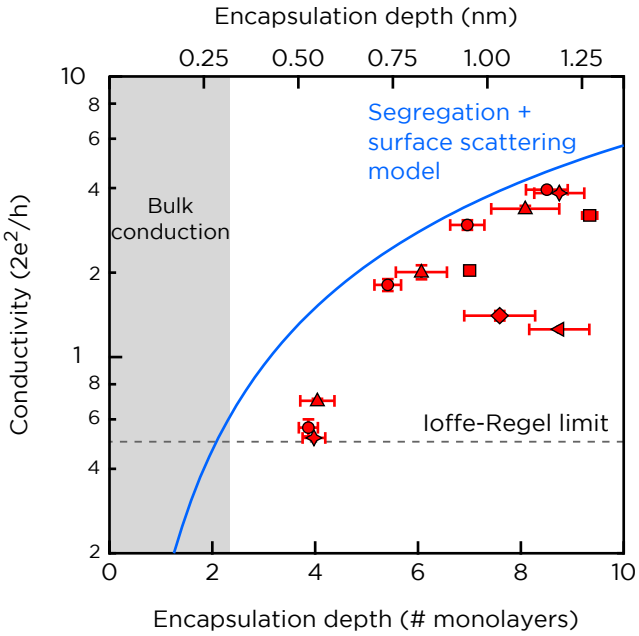


Figure 4.20: **Conductivity measurements at the shallowest depths.** A subset of all δ-layer measurements from this chapter with encapsulation depths of less than 10 monolayers (1 ML = 0.1358 nm). The shaded section denotes the depth range for which measurements have indicated bulk conduction (i.e. a resistance inversely proportional to probe separation), extending to a depth of 2 monolayers. The shallowest depth for which measurements have indicated 2D conduction (resistance independent of probe separation) is 4 monolayers, with the true limit presumably somewhere between 2 and 4 monolayers. The conductivity model from the preceding section is shown with the blue trace, and the Ioffe-Regel limit for metallic conduction in 2D is indicated by the dashed line.

4.4.4 Avenues for further refinement

The conductivity model presented in section 4.4.2 described the experimental data very well for depths of 2 nm and above. The small remaining error at the shallowest depths (most visible in Figure 4.20) suggests that the model can be improved by including additional physical effects arising close to the interface. Indeed, given the variety of complex interactions known to occur at the surface it is surprising that our simple model describes the data as well as it does. Here we will briefly discuss these additional effects.

Surface trapping of free carriers

We saw in section 4.4.2 that introducing a $1/d$ depth correction to the conductivity resulted in a greatly improved fit to the experimental data. An alternative means of introducing a 1/d factor is to consider the trapping of free charge at the surface, presumably by the same states responsible for Fermi-level pinning. If we consider the surface and the δ-doping layer to be pinned at different Fermi levels, we essentially have a fixed bias parallel plate capacitor, where the encapsulation layer serves as the dielectric. For

a given potential difference V, the amount of charge Q from the δ-layer trapped at the surface can be described by the familiar capacitor equation:

$$Q = \frac{\epsilon V}{d}$$

with ϵ the permittivity of the silicon encapsulation layer and d the encapsulation thickness. This would have a direct bearing on the free carrier density in the doping layer, but would also act to reduce the carrier mobility at the same time. Due to the extremely heavy doping in the δ-layer, the mobility and density of carriers are linked. The disordered Coulomb potential from the ionized dopant atoms results in severe impurity scattering, but this is partially screened by the large number of free electrons. Any process that removes carriers from the layer also reduces the screening efficiency and thereby reduces the carrier mobility [108].

Image charge effects due a dielectric mismatch

At the silicon-vacuum interface we have what is commonly termed a *dielectric mismatch* - the dielectric constant of the silicon substrate ($\epsilon = 11.7\epsilon_0$) changes that of vacuum ($\epsilon = \epsilon_0$) over the space of only a few nanometers [161]. This leads to image charges interactions, a well studied phenomena which leads to an *increase* in the ionization energy of dopants close to the interface [162;163;164;165;166;167] arising from the reduced screening of the donor potentials. If sufficiently severe this leads to dopant deactivation with a corresponding increase in resistivity. However experimentally it is typically seen that dielectric mismatch effects compete with opposing quantum confinement effects from the surface, which we discuss next.

'Hardwall' effects on the shape of the potential well

The silicon-vacuum interface effectively represents an infinite potential step, and for the shallowest depths being studied in this chapter this 'hardwall' potential step will have some bearing on the electrical properties of the donors. The potential well of the δ-layer will be modified from a symmetrical Hartree potential at large depths to a half-triangle, inversion-layer type potential due to the exclusion of the electron wavefunction from the half space outside the semiconductor. Such a change effectively increases the 'sharpness' of the well, which in turn alters the donor energy levels. As for dielectric mismatch effects, this is a well studied phenomenon in the context of single dopant atoms close to an interface and leads to a *decrease* in the ionization energy [164;165;166]. The final ionization energies of near-surface donors are thus determined by the combination of image charge and quantum confinement effects [162].The theoretical treatment required for a satisfactory account of these effects is beyond the scope of this chapter, but will be an important direction for future work.

4.5 Optimizing the resistivity of shallow δ-layers

In this section we investigate a method of achieving higher planar doping densities in the Si:P δ-layers, with the aim of improving the sheet resistance at shallow encapsulation depths. We will discuss and verify a method of nearly doubling the carrier density, then repeat the depth dependence four-probe measurements of the preceding sections. We demonstrate that the improvement in resistivity only becomes apparent for encapsulation depths $>$5 nm.

4.5.1 The chemistry of double dosing

Throughout this thesis we have been using a fixed process for creating Si:P δ-doping layers. Since a major theme of this chapter is the realization of low resistivity dopant layers at shallow depths, there is potentially value in exploring modified preparation 'recipes' to optimize sheet resistivities. In this section we will study a δ-doping sequence developed by McKibbin[168] which achieves a nearly doubled free carrier density.

In order to understand the modified doping sequence, we should first review the method used throughout this thesis. Phosphorus doping is accomplished by exposing a 2×1 reconstructed Si(100) surface to phosphine gas. The impinging phosphine molecules adsorb to silicon dangling bonds, automatically decomposing into phosphine fragments (PH & PH_2) by surrendering hydrogen atoms to adjacent dangling bond sites. The doping is self-limiting in that dangling bonds are required for phosphine adsorption, and these are eventually all occupied with PH_x and H species. Viewed in this way, the extent to which hydrogen occupies dangling bond sites is responsible for the limiting phosphorus coverage. In this section we will adopt an approach based on saturation dosing the surface with phosphine, heating the sample to selectively desorb hydrogen atoms and then phosphine dosing a second time. The process is thus:

1. Saturation dose a 2×1 reconstructed silicon surface at room temperature by introducing a phosphine pressure of 5×10^{-9} mBar for 5 minutes (1.4 L)

2. Anneal the sample with direct current heating to 550°C for 60 seconds, which removes adsorbed hydrogen but not phosphorus[169]

3. Allow the sample to cool to room temperature, then dose the surface again with 5×10^{-9} mBar of phosphine for 5 minutes (1.4 L)

4. Anneal the sample with direct current heating to 350°C for 60 seconds, incorporating the new phosphorus atoms

5. Encapsulate the sample with silicon as per the usual process

Henceforth we will refer to samples prepared by this process as *double dosed*, whilst samples prepared in accordance with the rest of this thesis will be referred to as *standard*. Low temperature Hall effect measurements (discussed in chapter 2) confirm the success of the double dosing method, as shown in Figure 4.21. Compared to a standard δ-layer, the double dosed δ-layer exhibits an 80% higher carrier density (3.75 $\times 10^{18}$ cm^{-2} vs. 2.09 $\times 10^{18}$ cm^{-2}) and an 84% higher sheet conductance (where the 4% discrepancy can be explained by a mobility improvement due to enhanced screening from the extra carriers).

It should be noted that double-dosed samples will be broader than standard layers due to the higher temperature annealing step. Earlier in section 4.2.0.3 we used an extrinsic diffusion model to predict that a 60 second 350°C anneal would broaden a δ-profile into a Gaussian of FWHM 0.003 nm; the same model predicts a Gaussian of FWHM 1.8 nm for a 60 second 550°C anneal[§]. Hence in terms of a comparative ultra-shallow junction plot such as Figure 4.13, the sheet resistance is reduced at the expense of a slightly larger *junction depth*. Without depth profiling such as APT or SIMS it cannot be definitively stated *how much* larger, but on the basis of the previous diffusion calculation we would expect a difference on the order of 1-2 nm. These depths remain highly competitive when considering the ITRS targets presented in Figure 4.13.

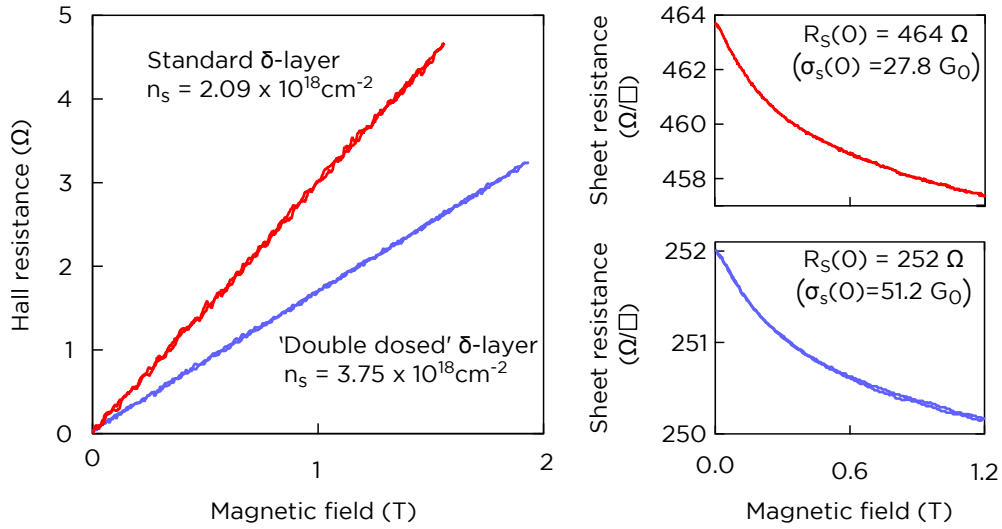


Figure 4.21: **Low temperature magnetotransport measurements of double dosed δ-layers** Hall effect (left) and magnetoresistance measurements for a 'standard' (red) and 'double-dosed' (blue) δ-layer sample. The double dosing procedure has increased the free carrier density by 80%, with a matching improvement in the conductance. Measurements are performed at 4 K.

[§]Since dopants are initially on the surface and can only diffuse in one vertical direction, the half-width-at-half-maximum of 0.9 nm is perhaps a more meaningful quantity

4.5.2 Depth dependence measurements

In Figure 4.22 we show the depth-dependent conductivity of double dosed and standard samples, where each marker shape corresponds to a unique sample (2 double dosed and 6 standard samples). At the deepest encapsulation depths the improvement in conductivity for the double dosed samples is obvious. However below ≈5 nm the different sample types exhibit essentially identical conductance. The cause of this behaviour is not clear; it may be that at these small depths the factor of ≈1.8 improvement in conductivity is dwarfed by much stronger effects close to the surface (such as roughness scattering or dielectric mismatch effects). A necessary next step for future work is to obtain SIMS or APT depth profiling of these samples to accurately account for the segregation profile using the conductivity model outlined in this chapter.

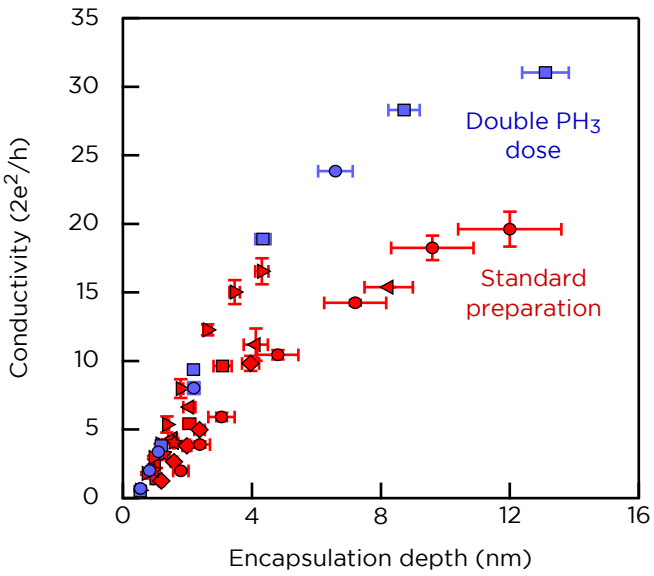


Figure 4.22: **A comparison of the depth-dependent four probe conductivity of standard and double dosed δ-layers** Room temperature *in situ* four-probe measurements demonstrate that while 'double dosed' samples (blue) generally have improved conductivity compared to 'standard' samples (red), this is not the case for encapsulation depths below ≈5 nm.

4.6 Conclusions and outlook

In this chapter we have employed the understanding gained from chapter 3 to study δ-doping profiles in silicon as a function of their vertical distance from the silicon-vacuum interface. With a combination of detailed *in situ* electrical characterization and high resolution depth profiling, we demonstrated that low temperature δ-doping in silicon is capable of creating 'ultimate' ultra-shallow junctions. While phosphorus dopants incorporated into only the topmost layer of the silicon lattice were not electrically active, we

observed Ohmic conduction after growing only 0.5 nm of silicon, with the ≈24 kΩ/□ resistivity then sharply decreasing with depth until saturating at ≈550 Ω/□ for depths beyond approximately 20 nm. The measurement results we present surpass all previous literature reports in terms of both resistivity and junction depth, and satisfy all currently projected ITRS targets. By studying these layers as a function of depth in high resolution, we have shown that a conductivity model incorporating a finite segregation length of the δ-layer combined with Fuchs-type surface roughness scattering can account for most of the observed depth-dependence behaviour. For encapsulation depths below 5 nm we have shown that additional interactions with the surface become important, and have indicated potential extensions to the conductivity model for future work.

What avenues for future research can be foreseen?

1. The resistivity of the δ-layers at shallow depths was shown to be primarily limited by the segregation length. As such, efforts to reduce segregation by altering the fabrication sequence (for example with different silicon growth rates or a dual-temperature encapsulation scheme[170]) could yield dramatic improvements to the already impressive depth dependence shown here.

2. There is scope for our conductivity model to be refined by including effects such as charge trapping and image charge interactions. Temperature dependence data taken at a series of different encapsulation depths would prove helpful in constructing a more complicated model. A refined understanding of the important effects at sub 5 nm depth may also explain the double dosing results, where we saw a smaller than expected improvement in the conductivity at very shallow depths.

3. It would be interesting to repeat these depth-dependence measurements on more commercially standard (i.e. heavily doped) substrates. As we noted, this may require the adoption of junction photovoltage measurements, since we saw in chapter 2 that the four-probe technique lost surface sensitivity on highly doped substrates.

A journal article encompassing the results of this chapter is currently in preparation. An additional manuscript regarding the double-dosing technique is also being prepared by McKibbin, and will include the measurements we have shown here.

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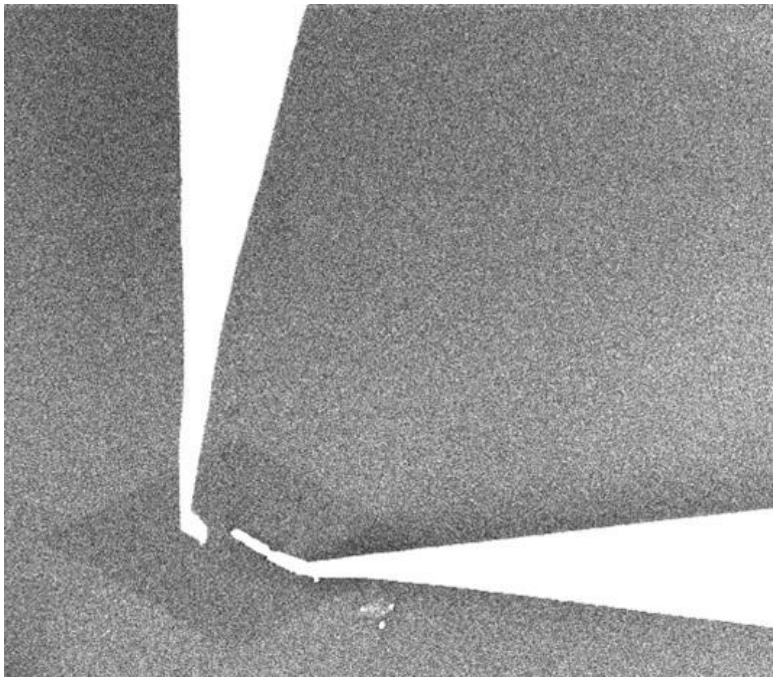


Nanoprobing patterned Si:P dopant structures

Index of key results and discussions

Background information about the motivation and challenges of measuring sub-micron scale patterned structures is given in section 5.1. Discussion about SEM contrast of delta-doped regions can be found on page 138.

Measurements of trench isolated regions of a Si:P δ-layer are shown in section 5.2 on page 144. It is seen that current injected into a δ-doped region does not spread into the surrounding substrate, an important result for more complicated measurements.

In section 5.3 we review the experimental methods for performing STM- and SEM-hydrogen lithography. We then use these techniques to measure micron-scale δ-doped patterns, with both single-probe (section 5.3.1) and multi-probe (section 5.3.2) electrical measurements. We do not observe Ohmic conduction, and on page 158 speculate on why this might be and how to proceed in future.

5.1 Introduction

In this section we review the motivation for measuring STM patterned dopant structures *in situ*, and discuss the major challenges we face in a transition to measuring patterned structures: seeing the structure in order to contact it, and reliably placing probes on structures less than a few square microns.

5.1.1 Why measure patterned structures?

In the preceding two chapters we have been using the Nanoprobe system to measure semi-infinite structures, both 2D and 3D. While such measurements are clearly not trivial and yield interesting results, they do not fully capitalize on the independence of the four probes. The ability to freely position the four probes enables the measurement of samples with small-scale features. The most prominent example of this is the characterization of nanowires, for which there is a considerable body of literature using similar four-probe systems.[171;172;173;174;175;176;177;178;179;180;181;182].

Given the potential of the hydrogen resist STM lithography technique, combined with the ability of the Nanoprobe system to both measure and modify surfaces *in situ*, one can envision many possible experiments:

- Extending the work of the previous chapter to studies of shallow dopant wires[9], or even dangling bond wires[183]
- Performing scanning tunneling potentiometry[184] on a nanoscale device while it is biased, with possibilities such as directly measuring the electric field distribution in a tunnel gap
- Creating a pattern such as a tunnel gap and measuring its transport properties as the gap region is modified (for example, selectively creating dangling bond sites in the gap).
- Creating and operating dangling-bond logic gates[16]

While there is hence tremendous potential, there are at the same time significant new challenges when compared with the work of the preceding two chapters. When measuring the δ-doped layers in chapters 3 & 4, we needed to ensure accurate *relative* probe positioning (i.e. equidistant spacings) but not *absolute* positioning on the sample. Similarly, we could avoid placing the probes especially close together.

In this chapter we begin the formidable task of measuring near-surface, lithographically patterned dopant structures. In this preliminary section we will briefly outline the

new challenges which are introduced, and how these can be addressed for the work of this chapter.

5.1.2 The problem of seeing what you're contacting

The first issue is how to contact a buried dopant pattern which, *a priori*, we may not expect to be visible to the scanning electron microscope used for positioning the probes. When the patterned structure resides on the silicon surface, the probes can in principle be operated in STM mode to locate the device*. However, as we have seen in the preceding chapter some level of overgrowth is required to electrically activate dopants. Once overgrown, STM imaging is no longer a viable means of locating the structure.

In chapter 2 we alluded to the use of etched registration markers to provide some means of identifying the absolute position of a patterning step[19;21]. For the experiments in this chapter we employ this technique; an example of the smallest etched features (line width ≈3 μm) is shown in Figure 5.1a. Simply observing the position of the STM probe relative to the markers during the patterning stage provides the location of the pattern to within ≈1 - 2 μm. However since we ultimately require sub μm positioning accuracy, this technique alone is not sufficient.

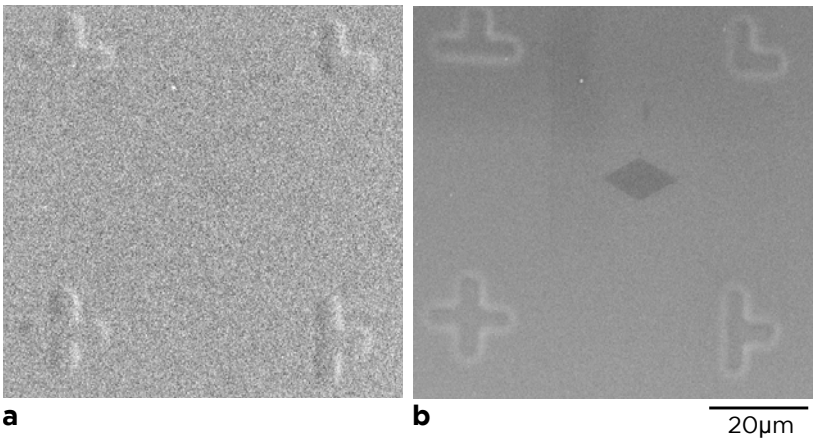


Figure 5.1: **Dopant contrast at shallow encapsulation depths under *in situ* SEM** Immediately after performing hydrogen lithography, the patterned region cannot be identified with the *in situ* SEM (a). After dosing the surface with phosphine, incorporating the dopants and encapsulating with ≈5 nm of silicon, the patterned region contrasts strongly with the surrounding substrate (b). Images are acquired with an in-lens secondary electron detector, at a beam acceleration voltage of 15 kV and working distance of 11 mm.

Fortuitously, imaging of buried dopants at these shallow depths is indeed possible with an *in situ* electron microscope. A much discussed yet poorly agreed upon phenomenon is that of *dopant contrast* under SEM observation - buried n-type dopants appear

*Such a procedure would require STM control electronics for all four probes, which we do not currently possess

darker while p-type dopants appear bright[185;186;187;188;189;190;191]. This difference in contrast corresponds to a lower secondary electron yield (for the case of dark regions), but the mechanism for this reduced yield is not universally agreed upon and may even arise by several quite different mechanisms. However a generally agreed upon observation is that the electron yield scales logarithmically with the doping concentration, strongly suggesting an electrical origin for the effect.

The samples in this chapter are unique for being both created and observed in a clean, UHV environment. This rules out proposed mechanisms involving surface contamination layers. We believe the most plausible explanation in this case to the strong internal band-bending in the sample, following from the theory of Volotsenko[186]. As discussed in chapter 3, lightly doped Si(100) substrates (both p- and n-type) exhibit downward band-bending near the surface due to Fermi-level pinning. This results in a surface electric field directed out of the sample, acting to increase the secondary electron yield (Figure 5.2a). In contrast, after δ-doping the extremely high density of phosphorus ions results in a strong attractive electric field (Figure 5.2b). This serves to retard secondary electrons exiting the sample, reducing the secondary electron yield and hence appearing dark in an SEM image.

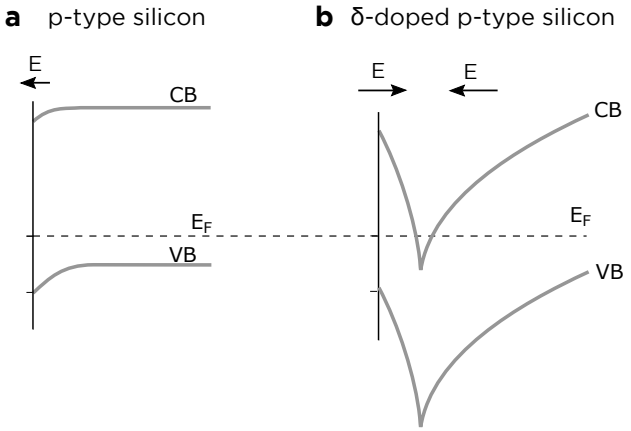


Figure 5.2: **The origin of dopant contrast in SEM.** Si(100) substrates have a Fermi level pinned to ≈0.4 eV above the valence band maximum (a), creating an electric field directed out of the sample which assists with the ejection of secondary electrons. In contrast a δ-doping plane induces strong band bending due to the dopant layer (b), with a resulting electric field which retards secondary electron emission and thus appears dark under SEM. A p-type substrate is shown, but the conclusion also holds on n-type substrate.

5.1.3 The problem of placing the probes

Once we know precisely where on the sample we need to place a measurement probe, we encounter the issue of how to do this at very small length-scales. The interesting measurement possibilities discussed earlier all assume nanometer scale structures, in which

case there are particular requirements for the measurement probes..

Probes must firstly be sharp in order to guarantee *placement accuracy*, where sharp means possessing a contact radius comparable to, or smaller than, the region of interest. For example, it is clear that none of the probes in Figure 5.3a are sharp enough to unambiguously contact a 50 nm wide wire structure. Larger micrometer-scale contact regions can be patterned to accommodate measurement probes, but the maximum size of these is limited by practical constraints. The STM desorption technique, while offering atomic scale resolution, is slow and not well suited for large-area patterning - desorption areas in excess of 10 μm $\times$ 10 μm would take several hours. Beyond simply having confidence that contact is being made in the right place, probes which are much larger than the feature of interest will be *invasive*. They will influence the system they are measuring, for example by shorting out the region being measured or by altering the dielectric environment. For cases where all four probes must be placed very close together, we also encounter issues with crowding. The probes in Figure 5.3b cannot be brought any closer together without contacting each other, limiting the minimum contactable feature size.

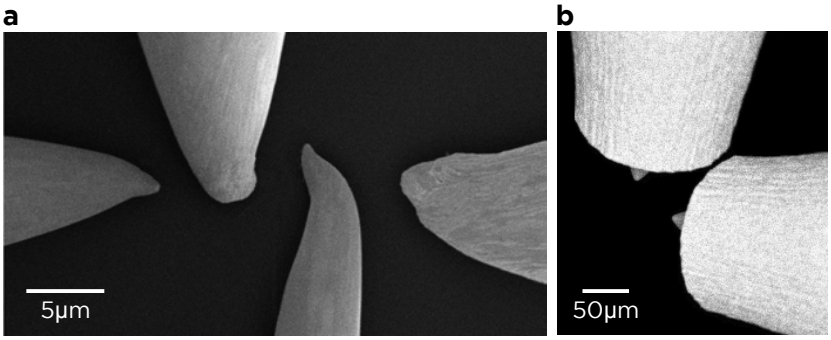


Figure 5.3: **The importance of micro- and macroscopic probe sharpness.** To reliably contact a small feature, we must use probes comparable to or smaller than the region of interest. Probes which are too large (a) will cause ambiguities in the precise point of contact as well as influence conduction through their (metallic) presence. Probes with inappropriate macroscopic shape (b) present different issues, in this case the inability to contact small features due to crowding.

There are further issues relating to the macroscopic probe shape which limit the reliability of accurate probe placement, as indicated in Figure 5.4. The overhead view afforded by the *in situ* SEM can be deceiving. In Figure 5.4b the probe has insufficient taper, and when mounted at an angle to the surface (required for multi-probe measurements) the lowest point of the probe is not at the apex. In Figure 5.4c the probe has some curvature, so again the lowest point of the probe is not the apex. However at the same time, very sharp probes are mechanically fragile. Close to the apex, they can effectively be considered nanowires, and are easily bent during a measurement. Once bent, the point of contact becomes ambiguous (Fig 5.4c).

Taken together, it is clear that there are very stringent requirements for satisfactory

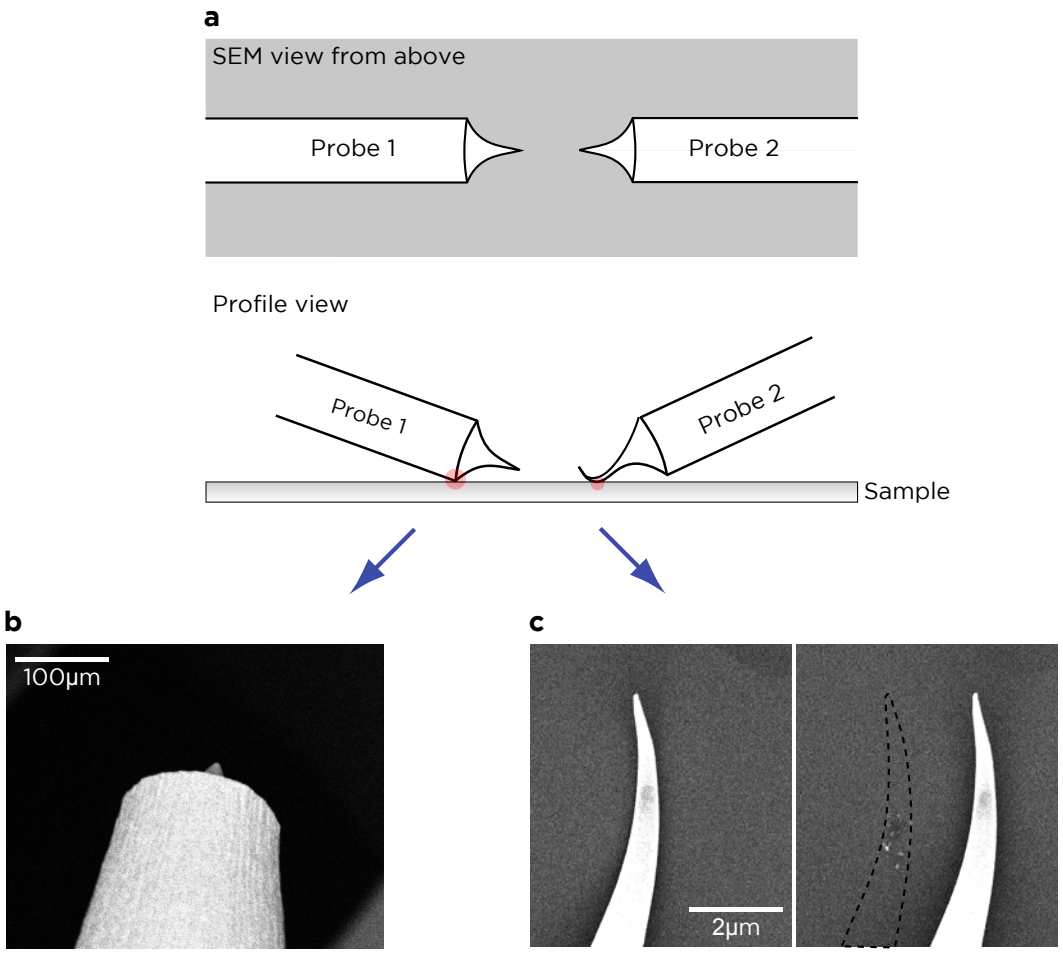


Figure 5.4: **Misleading artifacts arising from macroscopic probe shapes.** For a multi-probe measurement it is necessary for the probes to be mounted at an angle to the sample surface, but the SEM observation is from overhead (a). This can lead to cases where probes that appear normal are not contacting the surface at their apex. Extreme examples are shown in (b) and (c).

measurement probes. An appropriate probe must possess:

- Contact radius smaller than the features being measured
- Macroscopic taper which is long enough to avoid crowding of the probes and also guarantee that when mounted on an angle, the probe apex is the lowest point.
- Macroscopic taper which is not so long that the probe becomes mechanically fragile and easily bent
- Little to no curvature of the probe close to the apex, to guarantee that when mounted on an angle the apex is the lowest point.

Creating probes which satisfy these conditions is possible with electrochemical etching[192;193;194;195;196], but as evidenced by the unending stream of tip-etching papers in the literature there is no universally agreed upon 'best method'. In *Review of Scientific Instruments* alone there has been an article about electrochemically etching tungsten tips nearly every year for the last *25 years*[197;198;199;200;201;202;203;204;205;206;207;208;209;210;211], which serves to demonstrate that the straightforward, reproducible creation of 'perfect' probes is not a solved problem. For the measurement probes in this thesis we employ the lamella etching technique, where a small amount of electrolyte is suspended by surface tension inside a metallic ring (similar to the technique for creating bubbles from soapy water). The wire to be etched is threaded through the ring, and a bias applied between the wire and the ring. The resulting electrochemical reaction consumes the wire until it eventually becomes so thin that the lower section breaks off under the force of gravity. Ideally some control electronics detect this breakage and immediately shut off the bias to avoid further etching (and thereby blunting) of the wire. For this purpose we use the commercially available W-Tek control system from Omicron GmbH.

For the work in this chapter where it is critical to have sharp probes, we instead catch the part of the wire that falls. For this piece the bias voltage is removed *immediately* after the wire breaks, without requiring complex control electronics and guaranteeing the sharpest probe possible. Control of the macroscopic shape can then be obtained by varying parameters such as the electrolyte type and concentration, bias voltage or motion of the wire during etching. We typically use polycrystalline tungsten wire with a PtIr counter-electrode ring. The electrolyte is NaOH (16 g in 100 ml) with an applied bias of $\approx$6 V. In practice we find the final probe geometries to be highly erratic and only weakly dependent on the etching parameters. To obtain a sufficient number of probes suitable for measuring very small features, we simply etch batches of $\approx$30 probes and image them with an electron microscope to identify promising candidates (typically $\approx$ 70% of the probes are eliminated at this stage).

An alternative, unconventional approach to obtaining suitable probes involves appending a nanowire to the end of an electrochemically etched probe. This has been demonstrated with platinum coated tungsten oxide nanowires[179] and PtIr coated carbon

nanotubes[173]. The fabrication process for such probes is not trivial, but such a technique is necessary to achieve the full potential of a multi-probe system when measuring on sub 100 nm length scales.

5.1.3.1 The problem of non-destructive measurements

Assuming that we know where the probes must be placed and we possess appropriate probes, the final challenge is to non-destructively approach our highly fragile probes to the highly fragile sample surface. While non-destructive approaches are always desirable, in the previous two chapters it was always possible to simply move to a different location on the sample. When measuring a dopant structure, there is only one region of interest and typically only one set of probes, and a single over-approached probe will prematurely end an experiment (Figure 5.5 shows an extreme example of an over-approach).

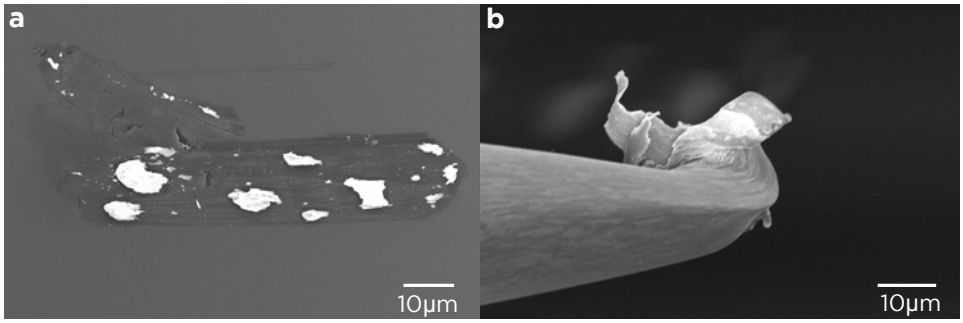


Figure 5.5: **Crashed probes ruin experiments.** An extreme example of a probe which has failed to detect surface contact while auto-approaching. Over-approaches are seldom this severe, but will still destroy both the region of interest (a) and the probe (b).

A common technique in the literature is to monitor the secondary electron shadow as seen by an off-axis detector[212] (Figure 5.6). In the absence of such a detector, in this chapter we instead rely on optimized parameters for standard electrical approaches. This involves using very high biases (≈-6 V) with low tunnel-current setpoints (≈200 pA) and small coarse-approach piezo steps. This leads to highly conservative (but very slow) probe approaches.

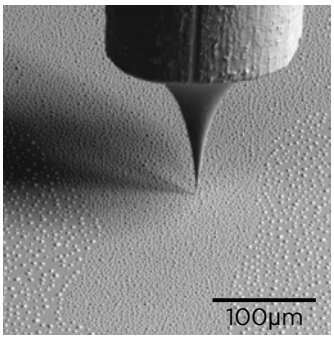


Figure 5.6: **Using the secondary electron shadow to approach a probe.** A common technique for probe approaches is to observe the secondary electron shadow seen by an off-axis detector. (*Adapted from Emundts et al*[212])

5.2 Coarsely isolated structures

Transitioning from the measurement of δ-layer samples to patterned dopant structures introduces several unknowns at once. A practical first step towards this goal is to coarsely isolate large sections of a δ layer. This allows us to study the electrical coupling between patterned dopant regions and the substrate while side-stepping issues relating to probe size and placement.

As discussed in the previous section, in order to measure small-scale patterned regions there are new challenges to be overcome regarding the measurement probes. We showed that these are technical problems with known solutions, and while they make measurements significantly more difficult, with due care they can all be addressed. However there are also new questions to address regarding the coupling between patterned dopant regions and the substrate. In chapter 3 we saw that the four-probe measurements were only sensitive to the δ-layer and not the substrate, which could be explained in terms of spreading resistance and the substrate:δ-layer resistivity ratio. Now that we are progressing to small dopant patterns it is not obvious how the interaction between the substrate and δ-doped region will change. Essentially, our problem is determining whether transport will still be confined to only the dopant pattern.

A useful first step towards understanding measurements on micro- and nanometer scale patterned δ-doping regions is to measure much larger structures (hundreds of micrometers). This will still tell us about the coupling between the substrate and a heavily doped phosphorus region, while leaving the rest of the measurement unchanged from those discussed in chapter 3. In this way we introduce the effects of isolated-dopant regions *before* introducing the effects of small probe spacings.

5.2.1 Experimental method

The 'lithographic' technique we will employ is to use an *ex situ* wafer scriber to trench isolate sections of a δ-doped sample, as indicated in Figure 5.7. Whilst not an especially high resolution technique, it is sufficient for these experiments and is also cleaner than wet chemical etching - the latter process would require spin-coating the surface with a polymer resist. The substrate in these experiments is 7 Ωcm n-type Si(100). The δ-doping procedure matches that of the previous chapters, with the exception that the encapsulation depth is increased to ≈20 nm in order to protect the dopant layer during the *ex situ* processing stages. Four-probe measurements performed before removal and after reloading confirm that the δ-layer is indeed unaffected (Figure 3.31 in chapter 3).

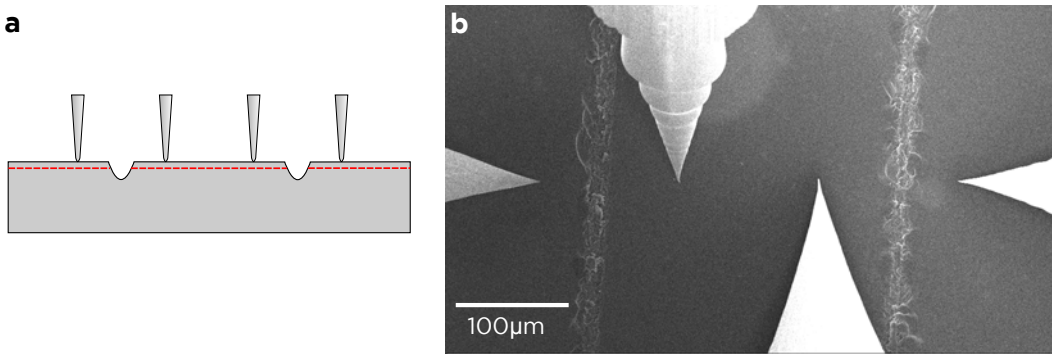


Figure 5.7: **Experimental method for measuring coarsely isolated dopant structures.** A uniformly δ-doped sample is scribed to trench isolate sections of the δ-layer (a). Subsequent collinear measurements across these trenches (b) provide information about the electrical coupling between the δ-layer and the substrate.

Care was taken while scribing to ensure that the trenches completely isolated adjacent sections of the δ-layer and extended across the entire width of the sample. As can be seen in Figure 5.7b, this meant obtaining scribe lines approximately 15 μm wide, with the desired removal of material within the lines. Immediately prior to UHV re-entry, the sample was chemically cleaned and HF etched to remove the native oxide. Once back in UHV no further heating or cleaning treatments were performed.

5.2.2 Measurement results

After reloading scribed samples into UHV, standard collinear four-terminal measurements were made with the probes straddling scribe lines as indicated in Figure 5.7. Representative results of such measurements are shown in Figure 5.8. We note that the experiment was repeated several times and the results found to be reproducible.

Each row (a-d) of Figure 5.8 depicts a different measurement configuration, as depicted in the left-hand column. Each configuration is expected to result in a different current path, as schematically shown by the blue arrows. We first note that in all mea-

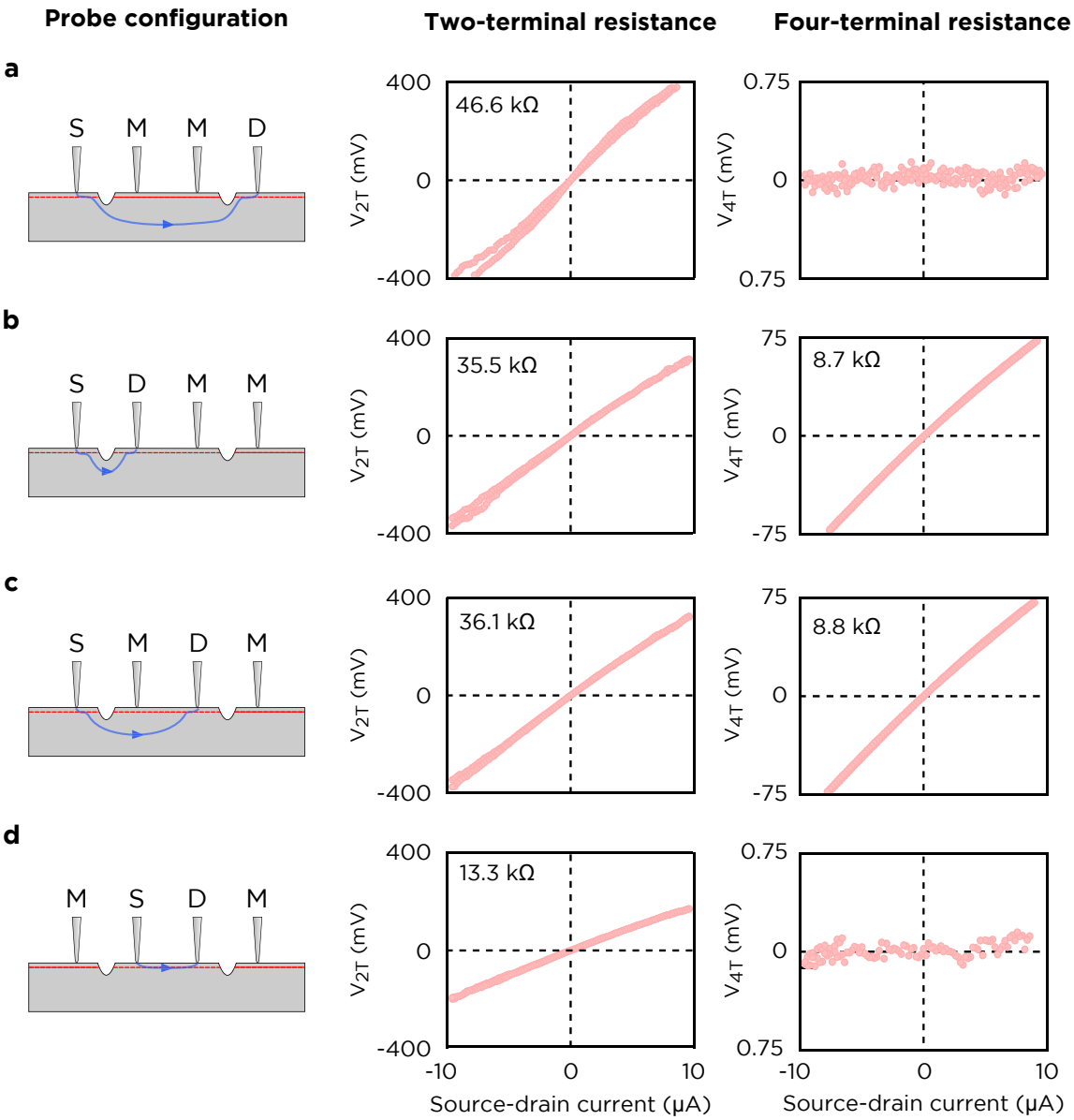


Figure 5.8: **Collinear four probe measurements on trench-isolated sections of a δ-layer** For all measurement configurations depicted (a-d) the two-terminal conduction is Ohmic. But surprisingly certain configurations (a,d) result in a four-terminal potential difference of zero, indicating that current does not spread through the entire sample.

surement configurations the two-terminal resistance is Ohmic or very close to Ohmic. It is not trivial to meaningfully interpret the values of two-terminal resistance (13 - 47 kΩ), since the symmetry of the potential distribution has been completely disrupted by the scribe lines. In one sense Ohmic conduction is expected, as the substrate is conductive at room temperature and each probe has an Ohmic contact to one of the sections of the highly doped δ-layer. However we note that this is the first time in this thesis that we have 'forced' current to leave the δ-layer, enter the substrate and then re-enter the δ-layer. Within the measurement range shown ($\pm 10\mu$A) there is no obvious barrier in this transport path.

The four-terminal resistances in the right-hand column provide an interesting insight into the electrical coupling between isolated sections of the δ-layer. In any configuration where the measurement probes do not share a section of the δ-layer with at least one source/drain probe (Fig. 5.8a,d), *no four terminal voltage exists!* Note that while the δ-layer is a metallic conductor, it is not a *super*conductor - the only possible way to obtain zero surface potential is for there to be no current carried in the δ-layer. The implication is that if current is not forced to enter or leave a section of δ-layer, it will not. For example, in Figure 5.8a current originating from the source probe is forced to enter the substrate in order to reach the drain probe. But the current is completely bypassing the trench-isolated section of δ-layer on which the two measurement probes are placed. Conversely, in Figure 5.8d the current travels from source to drain without ever having to leave the δ-layer and enter the substrate.

This is an encouraging result for our aim of measuring patterned dopant regions, particularly Figure 5.8d as this bears the closest resemblance to what we hope to accomplish later in the chapter. The implication is that if we position probes over an isolated δ-doped pattern, current will be contained within the pattern rather than spread throughout the conductive substrate.

5.3 Lithographically patterned features

Having shown preliminary measurements on coarsely isolated δ-doped regions and shown that current can be contained to within isolated δ-doped regions, in this section we discuss single- and multi-probe measurements of small scale (μm) *in situ* patterned dopant regions. Despite clear signatures of successful contact to the doped regions, Ohmic conduction through the δ-layer is not observed. We discuss possible reasons for this and outline plans for future progress.

It is clear that in order to reach the end-goal of measuring nanoscale dopant patterns

in situ, a more sophisticated patterning technique than wafer scribing is required. As discussed in chapter 2, the method of using hydrogen resist lithography as a means to perform selective doping on the Si(100) surface is proven and mature. In this section we will carry out multi-probe measurements of large-scale structures (several square μm) patterned with hydrogen lithography. This constitutes the penultimate step in the development of an *in situ* measurement process for atomic-scale dopant devices.

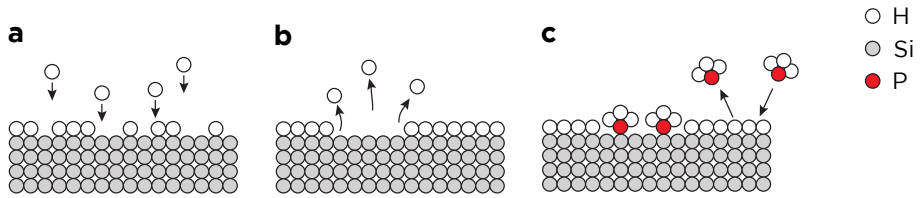


Figure 5.9: **Selective surface doping with hydrogen resist lithography.** A schematic representation of the hydrogen-resist lithographic doping scheme. The reactive Si(100) 2×1 surface is passivated by a monolayer of atomic hydrogen (a). With a controlled lithographic technique, select areas of the hydrogen resist are removed, re-exposing the reactive silicon surface (b). Phosphine gas now adsorbs only to the exposed regions of the surface (c).(*Adapted from Füchsle*[35])

We begin by briefly reviewing the experimental methods of hydrogen lithography. In the preceding chapters we have prepared semi-infinite δ-doping profiles by uniformly exposing a reactive silicon surface to phosphine gas. If instead we expose the surface to atomic hydrogen, (Figure 5.9a), a stable monolayer of hydrogen is formed, completely passivating the reactive surface. We obtain atomic hydrogen by connecting a molecular hydrogen leak valve to a thermal cracker. The hydrogen termination proceeds by heating the sample to 340 °C and dosing with hydrogen to a pressure of 5×10^{-7} mBar for 9 minutes, corresponding to an exposure of 200 L. This monolayer serves as a lithographic resist, blocking the absorption of phosphine. As a consequence, by selectively removing sections of the monolayer (Figure 5.9b), we enable selective adsorption of phosphine ((Figure 5.9c).

For the experiments in this section we are interested in large-area desorption, and employ two different methods suitable for this task: electron emission from an STM tip and indirect (Auger) excitation by a scanning electron microscope.

5.3.0.1 STM desorption of hydrogen

The highest resolution and consequently most popular method of lithographic hydrogen desorption employs the localized tunneling current from a scanning tunneling microscope[213]. In the low bias regime (<6 V) desorption to a resolution of single atoms can be obtained[23;214], making it an appealing technique for the creation of nanostructures. Operated in the high bias regime appropriate for large-area desorption, desorption rates on the order of $\approx$1 μm^2/h can be obtained with a resolution of $\approx$ 20nm.

As an example of this technique, in Figure 5.10 we show the edge of a large (2 μm $\times$ 3 μm) desorbed rectangle, created with a 7 V tip bias and a constant current of1 nA, at a rastering speed of 185 nm/s. The exposed silicon appears brighter than the surrounding hydrogen terminated surface due to the increased tunneling current through the surface states. (This image is obtained at a lower bias (2.8 V) and current (300 pA) which enables imaging without desorption).

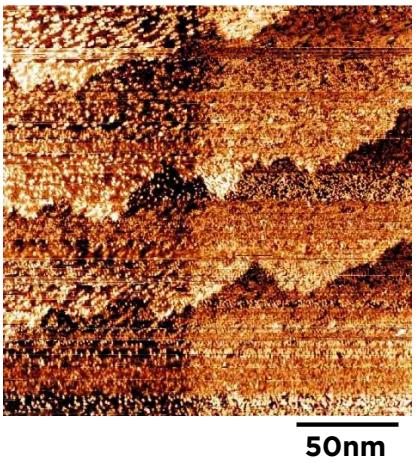


Figure 5.10: **STM-based hydrogen desorption** A close-up STM image of a desorption edge from a large-area rectangle pattern. The exposed silicon appears brighter due to the higher tunneling current obtained from the silicon surface states. Very sharp, well-defined desorption can be achieved with the STM technique.

5.3.0.2 SEM desorption of hydrogen

An alternative approach to hydrogen lithography is the use of an electron microscope, which can desorb surface hydrogen through an Auger process[215]. While the resolution ($\approx$100 nm) cannot compete with the atomic scale performance of STM lithography, the technique is nonetheless promising for a hybrid STM/SEM desorption scheme as proposed by Hallam *et al*. SEM desorption promises faster, more reliable desorption of large-scale areas, suitable for creating large area ($> \mu m^2$) contacts to STM patterned nanostructures.

For the measurements presented here, a 10$\times$10 μm square doped region was created by Huw Campbell as part of a larger investigation into optimizing the technique. After the standard sample preparation and hydrogen termination procedure, a 15 kV, 5 nA electron beam was rastered in a square pattern for 90 minutes, corresponding to a dose of $\approx$26 C/cm^2. Based on previous studies[38], this is expected to result in a phosphorus density of $\approx 1\times10^{14}$cm^2, with beam-induced carbon contamination of $\approx 2\times10^{12}$cm^2.

5.3.1 Single probe measurements

In chapter 3 we found it useful to approach four-probe electrical characterization by starting from single-probe current-voltage measurements. We will now take the same approach in our study of patterned dopant regions, and show that such measurements are useful for indicating whether a probe has successfully been placed on a doped region.

Several large-area rectangle patterns (henceforth '*patches*') were created by both SEM and STM desorption, ranging in size from (2 μm$\times$2 μm) up to (10 μm$\times$10 μm). The substrates were p-type (boron) with a nominal resistivity of (50 - 100) Ωcm. As the ability to measure small dopant regions was not obvious *a-priori*, these parameters were chosen in an effort to maximise surface sensitivity. On the basis of our findings in the previous chapter, an encapsulation depth of 6 nm was used for all samples. At this depth we expect the structures to be electrically active, but still close enough to the surface to be well coupled to measurement probes. The conditions for the phosphine dosing, incorporation and encapsulation were unchanged from all the previous samples we have discussed. All measurements presented here are performed at room temperature.

Before we examine I-V behaviour on patterned regions, it will be helpful to review the behaviour we observed in chapter 3 for the substrate alone and for a sheet doped (δ-layer) sample. In Figure 5.11 we reproduce measurements from chapter 3 on lightly doped p-type substrates. Measurements on the undosed substrate show three regions of differential conductance corresponding to series-resistance limited conduction (large negative biases), Schottky barrier limited conduction (small biases) and shunt-resistance limited conduction (large positive biases). We will refer to this collective behaviour as 'imperfect' diode conduction, where 'imperfect' implies deviation from the pure Shockley diode equation due to shunt and series resistance[94]. After δ-doping the Schottky barrier becomes extremely thin and hence transparent, simplifying the differential conductance to a higher, bias independent value. This corresponds to transport through the substrate with an additional, highly conductive transport channel.

In Figure 5.12 we show measurements of an STM desorbed patch (3.4 μm$\times$5.5 μm). The patch can be clearly resolved by electron microscope imaging (Fig. 5.12a), serving as evidence that the buried dopants are electrically active. The nature of the 3 dark regions (approximately 500 nm in diameter) is unclear; at this size the most likely candidate is tungsten clusters dropped from the STM probe during lithography (we note however that these should appear as bright rather than dark features). In Figure 5.12b we show two tip-to-sample I-V sweeps, with a probe located $\approx$20μm away from the patch (red trace) and then the same probe placed on the patterned patch (blue trace). We can verify the probe placement accuracy by the presence of a tungsten 'scuff mark' on the patch, approximately 200 nm $\times$ 500 nm in size (Fig. 5.12c). Here we have adjusted the contrast of the image to highlight this feature; a bounding box indicating the patch has been overlaid to indicate the relative position of the mark. The shape of the mark indicates that the

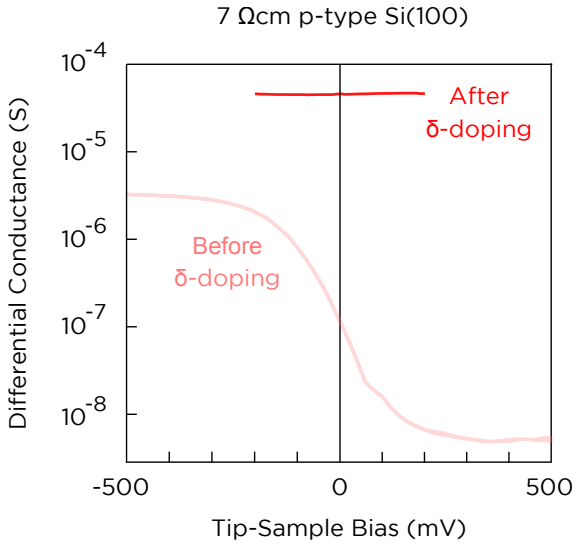


Figure 5.11: **Review of tip-sample conductance behaviour on lightly-doped and δ-doped substrates** As discussed in chapter 3, probe-to-sample conductance-voltage measurements provide useful qualitative information about the sample. Lightly doped substrates prior to δ-doping have the form of 'imperfect' diode conduction with three limiting bias regimes. After δ-doping the sample, rectification is eliminated and the conductance increases by several orders of magnitude.

probe made physical contact with the surface and then began to skid/slide as it was approached further.

The differential conductance traces in Figure 5.12b demonstrate an obvious difference between measuring on and off the patch. The off-patch trace (black) matches our 'imperfect diode' model of regular substrate measurements, with a small bias diodic region bounded by limiting shunt and series resistances at high biases. The measurements taken on top of the patch (red) introduce an additional plateau over the bias range of $\approx$ -60 mV to -480 mV. We find that this behaviour is reproducible - in Figure 5.13 we show similar measurements from a different sample in which we are able to place two probes on a patch. We see again that the additional plateau in the differential conductance appears when the probes are placed over a patch.

In order to discuss the origin of this conductance feature, we must first consider the possible contact mechanisms. In Figure 5.14 we show three possible scenarios:

- **Fig. 5.14a:** The probe physically penetrates through the patch, forming a Schottky contact with the underlying p-type substrate
- **Fig. 5.14b:** The probe forms a Schottky contact with the substrate, with the band-bending caused by the dopant patch serving to increase the effective barrier height of the Schottky barrier.
- **Fig. 5.14c:** The probe injects electrons into the dopant patch, which then recombine

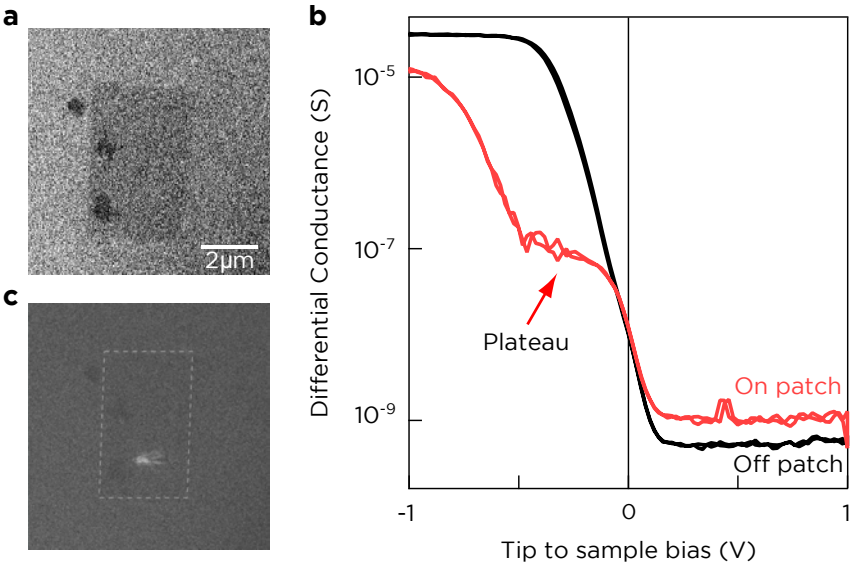


Figure 5.12: **Single probe I-V measurements on and off an STM patterned dopant patch** The 3.4 μm×5.5 μm STM-patterned dopant patch in (a) is clearly visible under the electron microscope, indicating electrically active dopants. Single probe-to-sample conductance-voltage measurements (b) show that a new electrical feature appears when the probe is positioned on top of the patch (red trace). In this case we could also double-check the placement accuracy by observing the location of a 'scuff mark' left on the sample surface after measuring.

with holes in the substrate.

Qualitatively, all three mechanisms will produce the same 'imperfect diode' conductance behaviour seen in Figure 5.11. While conceptually very different, Schottky contacts (Fig. 5.14a,b) and p-n junctions (Fig. 5.14c) share the same bias dependence of conductance, described by the Shockley diode equation discussed in chapter 3:

$$I(V) = I_S\left[\exp\left(\frac{\beta V}{n}\right) - 1\right]$$

$$G(V) = \frac{dI}{dV} = \frac{\beta I_S}{n}\exp\left(\frac{\beta V}{n}\right) \tag{5.1}$$

where $\beta = \frac{q}{kT}$ is the inverse thermal voltage, n the 'ideality factor' and I_S the reverse bias saturation current, which differs between Schottky and p-n junctions. The ideality factor essentially describes how well the data is described by the standard Shockley model; additional physical effects such as tunneling of carriers or generation-recombination in the depletion region can result in deviation from the simple exponential bias dependence (see for example p91 of Sze[110]). This is important to be aware of given that we are presently attempting to understand differential conductance traces with unusual structure. However such deviations from simple diodic behaviour only result in a 'kink' in the differen-

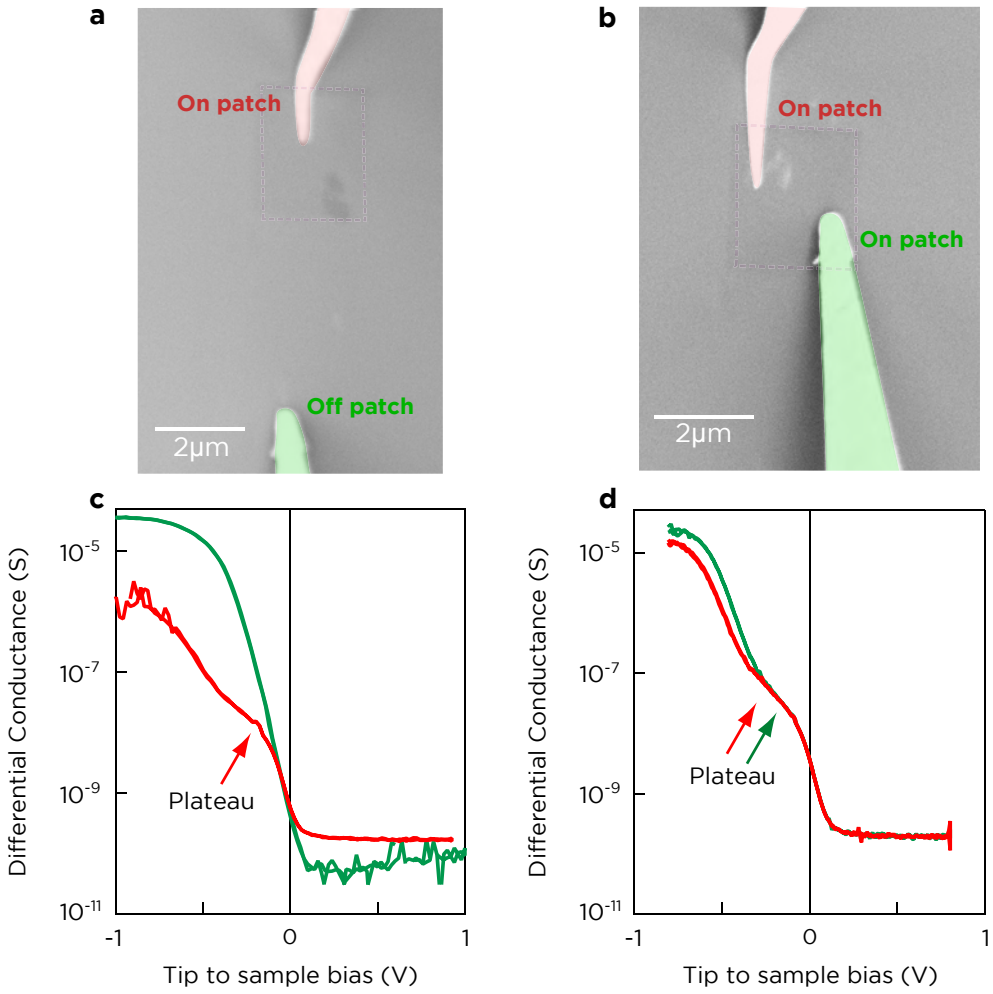


Figure 5.13: **Single probe I-V measurements on and off an STM patterned dopant path** Followup measurements on an STM-defined 2.2 μm$\times$3 μm dopant patch confirm the results shown in Figure 5.12 - when probes are placed on top of a dopant patch a plateau appears in measurements of the tip-to-sample conductance. The plateau is not present when the probe is positioned off the patch (a).

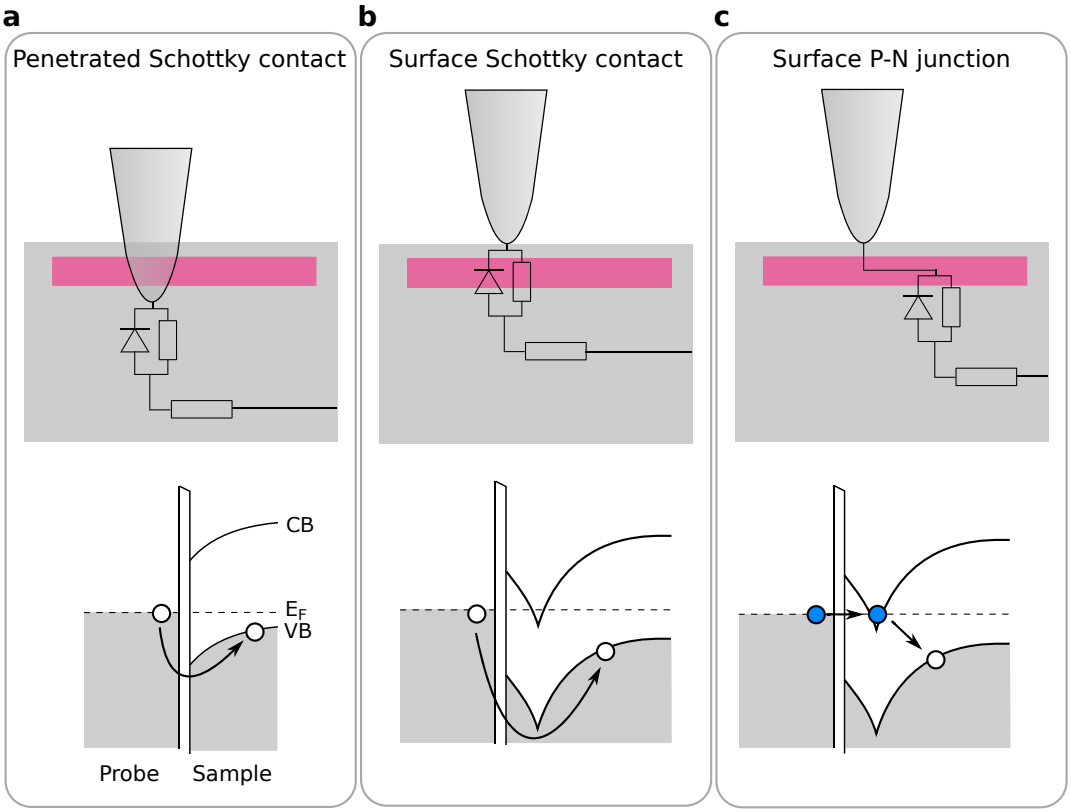


Figure 5.14: **Possible current injection mechanisms during single-probe current-voltage measurements.** A schematic depiction of three possible diodic current paths for a measurement probe contacting an n-type δ-doping region on a lightly doped p-type substrate. If the probe manages to penetrate deeper than ≈6 nm into the sample, a Schottky barrier to the substrate will be formed (a). If the probe does not penetrate the surface (b), a Schottky barrier to the substrate may form with a larger effective barrier height as holes must be excited over the potential well of the n-type δ-doping region. Finally, if electrons are injected into the well they can recombine with hole majority carriers in the substrate, a p-n junction (c).

tial conductance, and cannot account for a plateau as we see here.

There is no reason to expect that only *one* of the three current injection processes in Figure 5.14 will occur, and indeed the plateau feature observed in the differential conductance traces can be fully accounted for by considering two different diode elements in parallel. To see this, consider the equivalent circuit schematic in Figure 5.15a. With reference to Figure 5.15b, we can identify 5 different bias regimes in the conductance of this circuit as the tip-sample bias decreases from a large positive value:

1. Both diodes are fully reverse biased and do not conduct. Conductance is limited by the two shunt resistances in parallel

2. One of the diodes begins to conduct more than its shunt component, giving a net conductance with an exponential bias dependence

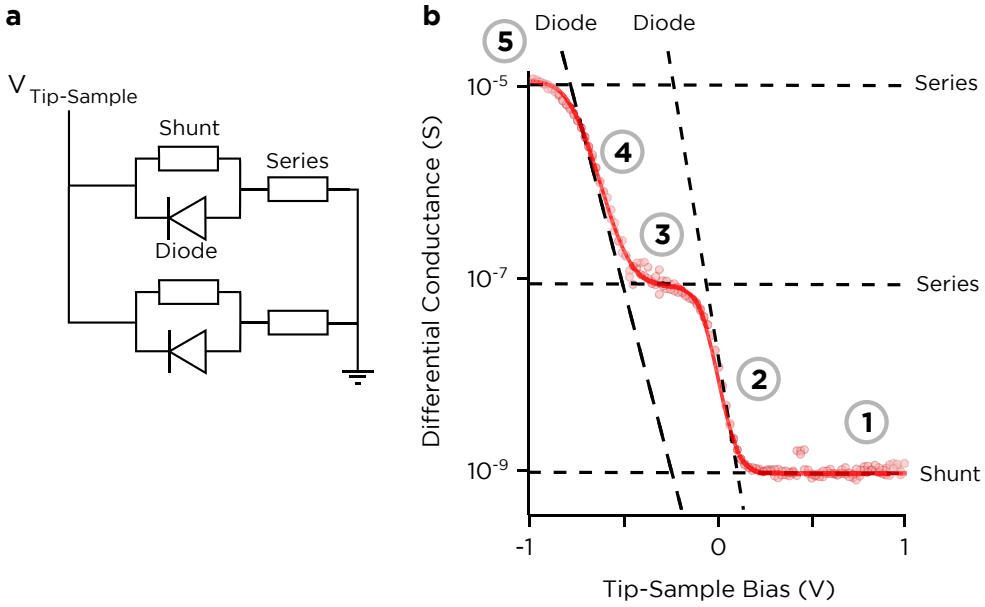


Figure 5.15: **A model for the plateau in tip-to-sample differential conductance measurements over a dopant patch**. A simple model encompassing two 'imperfect' diode pathways in parallel (a) can completely account for the plateau seen in experimental tip-sample conductance measurements (b). The numbered regions refer to the conduction regimes discussed in the text.

3. The conducting diode saturates, and the net conductance is now limited by the respective series resistance associated with that diode

4. The second diode begins to conduct more than its shunt component, making the conductance once more exponential with bias

5. The second diode saturates. Conductance is now limited by the two series resistances in parallel.

In Figure 5.15b we identify these regimes on the conductance data from 5.12. The solid line is a fit to the experimental data using the simple model of Figure 5.15a[†], and demonstrates that this simple interpretation can completely account for the differential conductance features.

What has been gained from building an understanding of these single-probe measurements? Chiefly, we have obtained the important qualitative observation that the appearance of a conductance plateau in a tip-to-sample I-V measurement serves as unambiguous confirmation that the probe is positioned over a patterned dopant region. In view of the discussion at the beginning of the chapter regarding the difficulty of accurate, reliable probe placement, this is an extremely useful result.

[†]The form of the fitting function consists of simple series and parallel combinations of the diode conductance given by 5.1 with the shunt and series conductances. The resulting expression is cumbersome, and it would not add to the discussion to write it out in full.

5.3.2 Multi-probe measurements

Having demonstrated an understanding of single probe measurements on δ-doped patches, we now turn to the main objective of this chapter - multi-probe measurements of conduction *through* these structures. This represents the final step in the development of an *in situ* measurement process - all that remains beyond this point are the practical experimental issues in down-scaling, which we discussed in section 5.1.

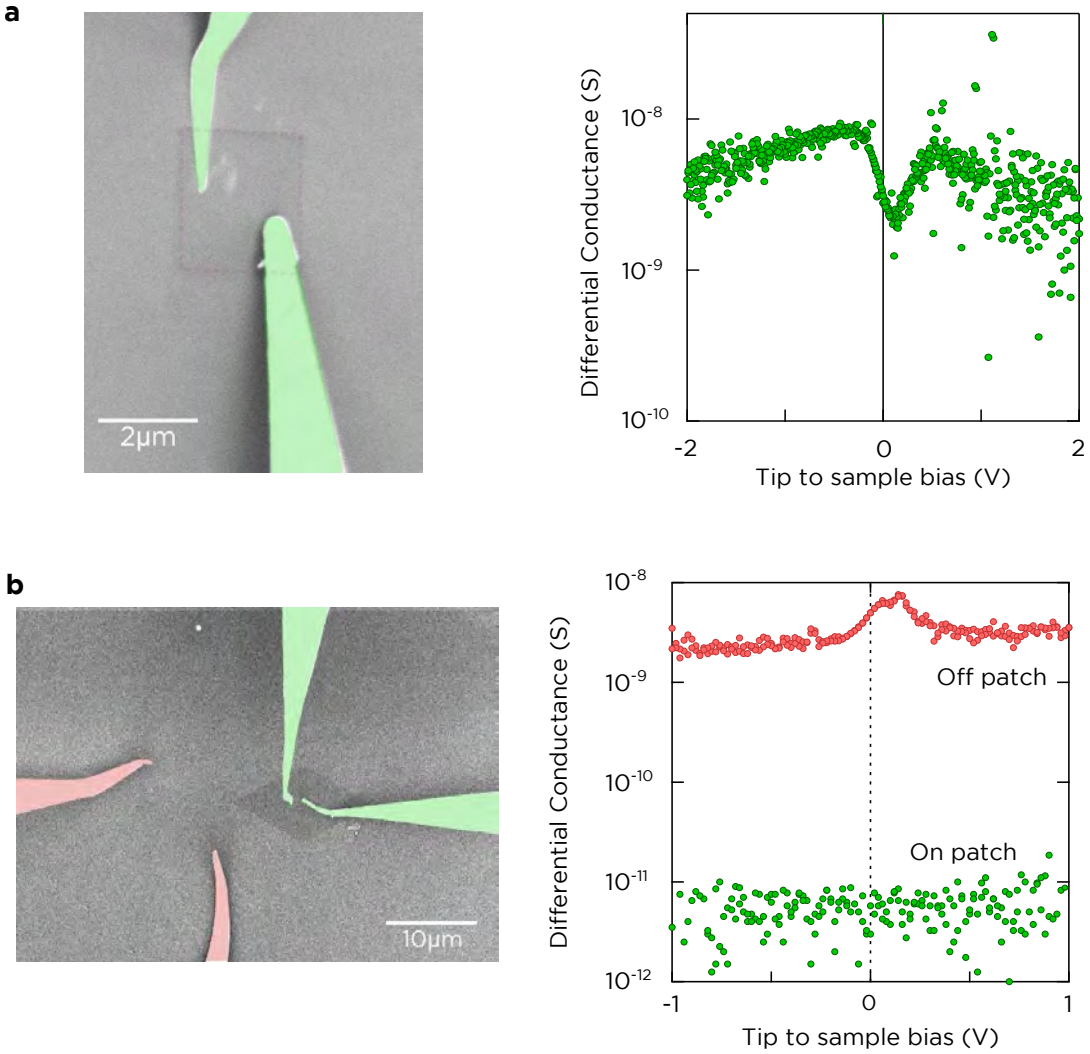


Figure 5.16: **Two-terminal resistance measurements of STM patterned dopant patches** Measurements on two different STM patterned dopant patches (a,b) do not demonstrate conductance commensurate with metallic conduction through a heavily doped region. In (a) the conduction through the patch is not Ohmic, while in (b) the conduction through the patch (green) is Ohmic but 3 orders of magnitude *lower* than the conductance measured off the patch (red).

In Figures 5.16 we show two-terminal resistance measurements of two different STM-desorbed patches, while in Figure 5.17 we show four-terminal measurements on an SEM-

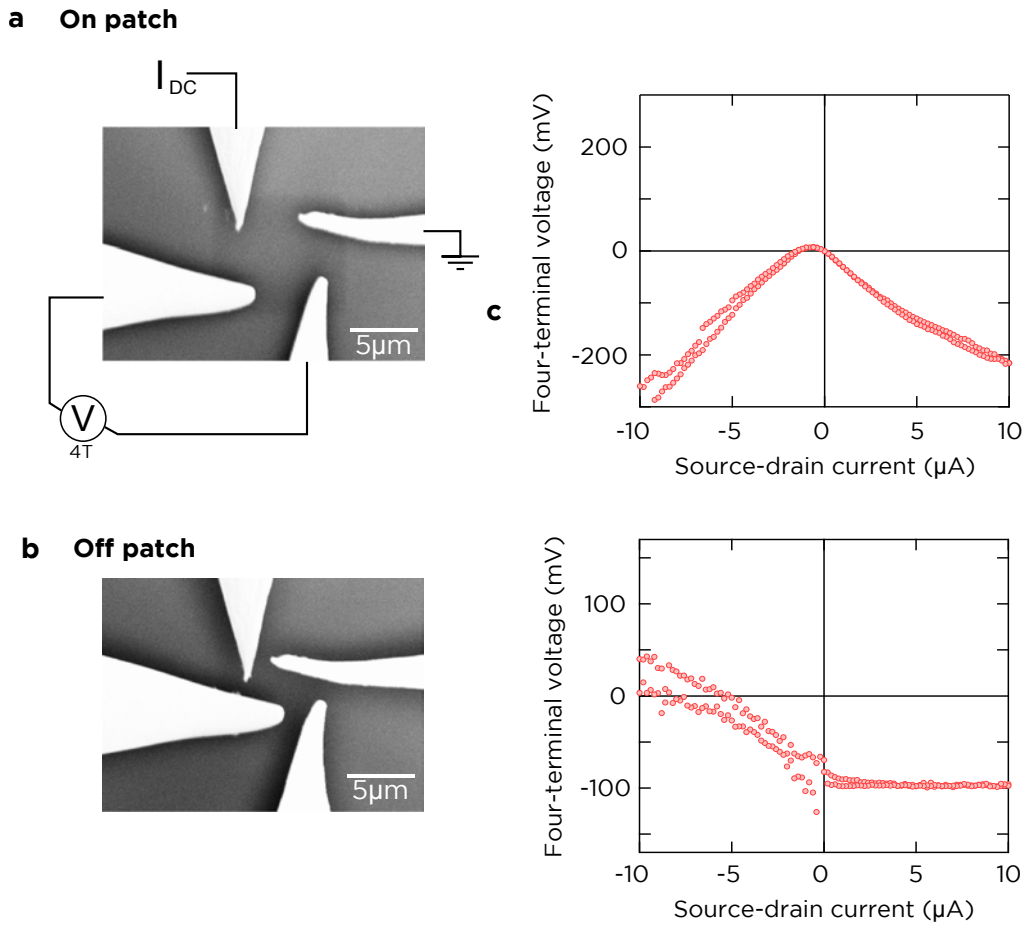


Figure 5.17: **Four-terminal measurements on an SEM patterned dopant patch** Four terminal van der Pauw resistance measurements on (a) and off (b) an SEM desorbed dopant patch indicate that the absence of metallic conduction seen in Figure 5.16 is not simply an artifact of the measurement being two-terminal. For the SEM desorbed patch the four terminal V-I traces are nonlinear and cannot be meaningfully interpreted as an Ohmic resistance.

desorbed patch.

Due to the relatively small areas available with the STM desorption technique combined with the difficulty of simultaneously possessing four perfect probes, at the time of writing only two-terminal measurements were obtained on the STM desorbed dopant patterns. For the SEM patch in Figure 5.17 we were able to place all four probes on the patch; in the interest of occupying the smallest area possible the well known van der Pauw measurement configuration was adopted[86].

In each case the placement of the probes was verified by the observation of the differential conductance plateau discussed in the previous section. Despite this, none of the measurements shown in Figures 5.16 or 5.17 exhibit the level of conductance we would expect from a δ-doped region. Indeed, only Figure 5.16b shows Ohmic conduction through the patch (green trace), but this is in excess of 100 GΩ, nearly 3 orders of magnitude *less* conductive than the comparable measurement taken *off* the dopant patch (red trace).

What can be said of this failure to observe Ohmic conduction? All of the desorbed regions show strong contrast under SEM observation, indicating that the dopants are present and electrically active. There is no question that patch structures of this size should conduct well (< 10 k$\Omega/\square$,[38]). As discussed in the previous section, we also have a means of ensuring that the probes are accurately placed. We see no fundamental reason for multi-probe measurements of dopant patches to be impossible, and in anticipation of future development it is worth considering potential causes for the behaviour seen here:

1. **The hydrogen desorption is incomplete, such that the density of incorporated phosphorus is much lower than expected.** An obvious possible cause of the poor conductivity we have seen here is simply that the patterned dopant regions are malformed in some way. Incomplete hydrogen desorption is unlikely given the very conservative desorption parameters coupled with STM imaging of desorption edges (Figure 5.9. Nonetheless, the logical next step is to independently test the electrical properties of the patterned dopant regions. This can be performed by *ex situ* transport measurements using lithographically patterned metallic surface contacts. Such experiments are underway at the time of writing.

2. **Something new happens at very small probe spacings.** Should the *ex situ* cryogenic measurements indicate that the patches are indeed electrically active and heavily doped, we will need to consider the possibility of new physics occurring at these sub-micron probe separations. An obvious example of this is the electric field established between two very sharp, very close probes, which may be sufficient to alter the electronic structure in the underlying sample. Since sharp probes are unavoidable, it may then be necessary to increase the patterning area to allow a larger probe separation.

3. **Surface sensitivity is lost at this scale.** A third possibility is that by severely reducing the dimensions of the 2D doping region, we have lost the surface sensitivity which we discussed at length in chapter 3. This could potentially be addressed by adopting fully depleted (i.e. very thin) silicon-on-insulator substrates, effectively eliminating the possibility of substrate transport. We note that employing the *in situ* cryostat to cool the sample would not be an adequate solution; we have shown in chapter 3 that at the minimum achievable temperature (≈35 K) the substrate resistivity is not appreciably higher while the δ-doping layer conductivity is improved by less than a factor of 2.

5.4 Conclusions and outlook

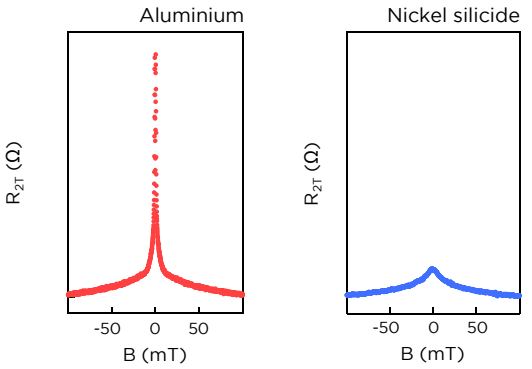
In this chapter we have made significant progress towards the goal of combining the *in situ* nanoscale four-probe characterization technique with the hydrogen-resist lithographic technique for creating nanoscale dopant structures.

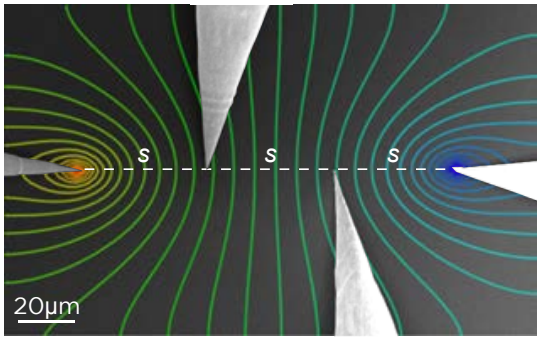
In section 5.2 we used measurements of coarsely isolated δ-doped regions to show that current injected into a δ-doped region does not spread into the surrounding substrate, even when using conductive substrates at room temperature. This provides an early indication that it is possible to measure lithographically defined heavy doping regions without being concerned about parallel conduction through the substrate.

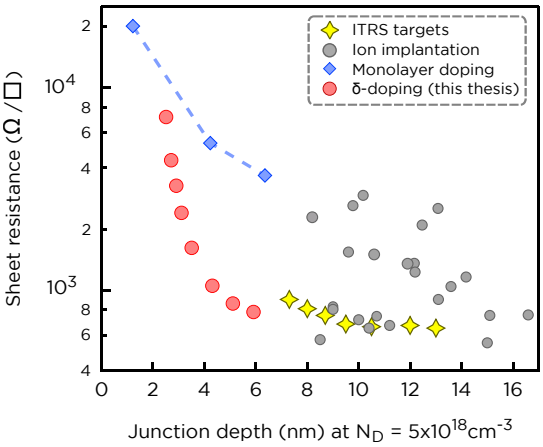
We then proceeded to lithographically pattern (with both STM and SEM desorption techniques) dopant patches several square microns in size (≈ 6 - 100 μm^2) and perform *in situ* electrical measurements on them. We were able to show that there is a clear electrical signature for probes placed on a dopant patch in the form of a plateau in tip-to-sample conductance-voltage measurements. We were able to interpret and model this behaviour in terms of a parallel diodic current path at the probe contact. This will be an invaluable technique for future four-terminal measurements when the accurate placement of all four probes must be verified.

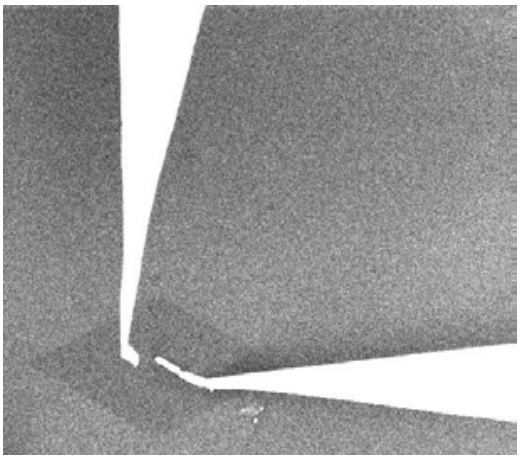
Finally, we were able to obtain preliminary two- and four-terminal *in situ* resistance measurements on patterned dopant regions. While we did not observe Ohmic conduction through these structures, a clear path was established for future work to demonstrate either that the experiment simply needs to be repeated or that new physical effects are occurring which will require a revised fabrication and measurement strategy.

We are optimistic that future work will be able to rapidly build upon the foundations in this chapter to realize the potent combination of an atomic-scale fabrication technique with an *in situ* electrical measurement technique, opening the door for a range of interesting and unique experiments.









Conclusions

In this thesis we have demonstrated advances in both *ex situ* and *in situ* measurements of Si:P δ-doped silicon. In particular, we demonstrated that a four-point-probe STM can be used as an accurate and unambiguous tool for characterizing the sheet resistance of planar, high concentration surface doping layers in silicon.

In Chapter 2 we developed a nickel silicide metallization scheme for making *ex situ* Ohmic contact to buried, highly doped Si:P devices. Without compromising the stringent thermal budget restrictions to avoid dopant diffusion, we were able to successfully replace the aluminium based scheme developed by Reuß. Through comprehensive comparative magnetotransport studies on aluminium and nickel silicide contacted Hall bar samples, we could show that the contact resistance is comparable for the two metallizations ($\approx$60 Ω), and that the use of nickel silicide does not contribute to rate dependent magnetic field hysteresis. Most importantly, the contact resistance artifact which arises when using aluminium contacts was shown to be eliminated by the use of nickel silicide.

In Chapter 3 we transitioned from *ex situ* to *in situ* contacting techniques, and developed an understanding of how a four-probe STM system can be used to unambiguously measure the sheet resistance of near-surface ($\approx$4 nm deep) Si:P δ-doping profiles in silicon. Given that direct-current heating is used to fabricate these samples and that probe-to-sample approaches employ electrical feedback, the use of conducting susbtrates is a requirement. Extensive investigation was required to establish confidence that measurements are not skewed by parallel leakage conduction through the substrate. Through thorough analysis of resistance measurements with varying substrate types, probe separations and sample temperatures, we built a compelling body of evidence that we are measuring solely the δ-layer, uninfluenced by the substrate. We proposed and experimentally verified that this could be explained by considerations of spreading resistance and the relative two-terminal resistances of the δ-layer and the substrate.

Having built this understanding and confidence regarding the characterization of shallow Si:P δ-layers, we then asked whether we could in bring these layers *even closer* to the interface, and what that would do to their electrical characteristics. In Chapter 4 we answered these questions, capitalizing on the possession of an all UHV fabrication and measurement technique to sidestep issues of surface oxidation or contamination. The ångstrom level of control afforded by our silicon sublimation source allowed us to study Si:P δ-layers over depths of 0 to 20 nm in sub-nanometer increments. This is topic of particular significance for CMOS scaling, where shallow doping is an integral part of planar transistor architectures. We found that the 'ultimate' ultra-shallow junction - a dense monolayer of phosphorus dopants incorporated into only the topmost layer of the silicon lattice - was not electrically active, in accordance with earlier studies (and arguably, common intuition). But surprisingly we observed the onset of Ohmic conduction through the layers at depths of only 0.5 nm (approximately 4 silicon monolayers), with the $\approx$24 k$\Omega/\square$ resistivity then sharply decreasing with depth until saturating at $\approx$550 $\Omega/\square$ for depths beyond approximately 20 nm. We were able to capture this behaviour with a

depth dependent conductivity model incorporating a finite segregation length of the δ-layer together with Fuchs surface roughness scattering. Importantly, the sheet resistances we obtain at the depths we obtain them surpass all currently projected ITRS requirements for ultra-shallow junctions.

Finally, in Chapter 5 we began to exploit the full power of the four-probe STM system by studying laterally patterned Si:P δ-doping regions made with a hydrogen lithography technique. We highlighted the daunting challenges this introduces, and provided means to overcome them. We gave experimental verification that current passing through an isolated dopant pattern at room temperature does not 'leak' through to the underlying substrate. After creating phosphorus doped planar 'patches' several square micrometers in size and $\approx$6 nm from the surface, we obtained one-, two- and four- terminal resistance measurements. From the one-terminal measurements we obtained a method of verifying tip placement accuracy by examining the tip-to-sample conductance traces on a logarithmic scale. A unique plateau feature at negative tip biases was shown to correlate with placement over a phosphorus dopant patch; we showed that an additional diodic current path can account for the appearance of this plateau. The two- and four- terminal measurements did not yield the level of Ohmic conduction expected on the basis of the δ-layer studies from previous chapters, but we could identify a clear path for future research to determine the cause. We will discuss this path in the following section. Most importantly, we still as yet see no fundamental reason for our eventual goal of measuring STM-patterned dopant devices *in situ* to be impossible.

Future work

With the main content of the thesis concluded, it is worthwhile reflecting on what has been 'left on the table' for future work. The initial difficulties of using and interpreting a *in situ* 4PP STM system for measurements of phosphorus-in-silicon doping structures now have been resolved, and we note two readily apparent directions in which to take it:

The continued understanding and optimization of near-surface Si:P δ-doping layers
In chapter 4 we investigated the depth dependent conductivity of Si:P δ-doping layers, with the UHV environment and controlled silicon overgrowth rate providing us with the ability to measure well-defined depths down 0nm in sub-nanometer increments. There are two directions in which this work can be extended:

1. *Investigation of surface effects on 2D dopant system:* We put forward a model for the depth-dependent conductivity based on segregation and surface scattering, and while this described much of the experimental data very well, it overestimated the conductivity at the shallowest depths. This indicates that additional physical effects should be included in the model, and we discussed the possibility that these might be image charge or surface bandstructure related. There is scope for future

work in developing a more complete physical model. Temperature dependent measurements as a function of depth may prove informative here, as will forthcoming scanning tunneling spectroscopy[155] and photoemission data[154]. Similarly, it would be interesting to determine more conclusively whether the 'threshold' depth of $\approx$0.5 nm for the onset of Ohmic conduction corresponds to something physically significant such as a transition out of strong localization, or whether it simply reflects a limitation of the experimental technique.

2. *Applications of shallow Si:P δ-doping in future CMOS nodes:* We noted that the sheet resistances we measured in chapter 4 were extremely competitive if viewed as ultra-shallow junctions. There are several easy steps that could be taken to make this comparison more robust. The foremost of these would be the use of more conventional highly doped (5×10^{18}cm^{-3}) p-type substrates. In our measurements on n-type substrates of this doping level in Chapter 2 sensitivity to the δ-layer was lost, but this may not be the case if measuring on an n/p doping structure rather than n/n. The inclusion of a complementary non-contact technique such as junction photovoltage may be useful for such measurements. To be serious about commercial integration of the technique, it will also be important to engineer a move to larger samples, and verify the uniformity of the doping layer over large length scales. The 2.5 mm$\times$10 mm samples we use in this thesis are quite far removed from a standard 12 inch wafer, but full size wafers will present new challenges with sample heating as direct current heating will no longer be possible.

   Viewed in an 'applications' context, shallow doping is very much a numbers game. Several obvious pathways to improving the depth dependent sheet resistivities are open for further study. In particular, we noted that at present the largest factor determining sheet resistance at shallow depths is the segregation length of the doping layer. The segregation length can be readily adjusted by tuning the growth rate and temperature. While it will be crucial to obtain guidance from SIMS or APT depth profiling in such an endeavour, we should not forget that an *in situ* measurement technique is now available as well. This reduces the length of the feedback loop from weeks to hours, the value of which cannot be overstated. Along similar lines, we also noted the improvement possible by variations such as 'double dosing' the surface with phosphine. There is much scope for the creative experimentalist to optimize the depth-dependent resistivity of the Si:P (and related) shallow doping systems.

2. *In situ* measurements of patterned dopant structures

In chapter 5 we started down the intriguing yet highly challenging path of combining the *in situ* four-probe measurements with the atomic-scale STM hydrogen lithography technique. We found two- and four-terminal resistance measurements of micrometer scale desorbed patches did not show conduction in the manner we expected. Once this

can be resolved the doors are open for a diverse range of exciting experiments. The specific experimental roadmap we envisioned to resolve the lack of conduction was as follows, with some of these underway at the time of writing:

1. *Ensure the patterned region is electrically active:* By creating sufficiently large area dopant patterns $>(10\mu\text{m}\times10\mu\text{m})$ it is possible to deposit *ex situ* metallic surface contacts on the sample following the completion of the *in situ* measurements. In this way it is possible to carry out low-temperature van der Pauw measurements to conclusively determine whether the dopants are electrically active. If not, time must be spent diagnosing problems with the lithography stage such as incomplete hydrogen desorption.

2. *Pattern much larger structures:* STM lithography is an unrivalled method in terms of atomic precision, but for structures on the micrometer scale it is very slow. Nonetheless, given that we are still in the developmental stage it is not unreasonable to carry out one-off large scale patterning steps ($20\mu\text{m}\times20\mu\text{m}$ or larger). In addition to greatly easing the task of contacting with four probes simultaneously, this would be a means of addressing whether something new is happening at very small probe spacings to influence the conductivity of the dopants (such as the effect of large electric fields)

3. *Transition to SOI substrates:* The final possibility is that by reducing the lateral dimensions of the δ-doped region to only a few micrometers, we have forfeited the surface sensitivity and are now strongly influenced by parallel substrate conduction. This could potentially be addressed by the adoption of fully depleted silicon-on-insulator substrates.

Appendix A: Deriving correction factors for 4-probe measurements

A.1 Potential distribution from a single tip

Consider a single probe contacting some laterally infinite medium of uniform resistivity. If we apply a fixed bias to this tip, a constant current will flow.

$$\nabla \cdot J = 0 \qquad \text{(constant current)}$$

We also assume that the sample obeys Ohm's law:

$$J = \sigma E \qquad \text{(Ohm's law)}$$

and note that the electric field E is the gradient of the sample potential:

$$E = -\nabla \Phi$$

Taken together, we have:

$$\nabla \cdot (\sigma(-\nabla \Phi)) = 0$$

By using a second derivative ∇ identity we can rewrite this as

$$\sigma \nabla^2 \Phi + \nabla(\sigma) \cdot \nabla \Phi = 0$$

But $\nabla \sigma = 0$ (uniform resistivity), and so:

$$\sigma \nabla \cdot (-\nabla \Phi) = 0$$

$$\boxed{\nabla^2 \Phi = 0} \tag{A.1}$$

Which has brought us to the **Laplace equation**. We will proceed by solving for Φ in different geometries, and then employing the resulting expression for the potential

distribution to evaluate a four-terminal resistance.

A.2 Φ on a 3-dimensional substrate

If a single probe on the surface injects a current into an infinitely deep substrate, by symmetry the current will spread out spherically from the tip. In order to solve equation A.1 we should therefore use spherical polar coordinates:

$$\nabla^2\Phi = \frac{\partial}{\partial r}\left(r^2\frac{\partial\Phi}{\partial r}\right) + \frac{1}{sin(\theta)}\frac{\partial}{\partial\theta}\left(sin(\theta)\frac{\partial\Phi}{\partial\theta}\right) + \frac{1}{sin^2(\theta)}\frac{\partial^2\Phi}{\partial\phi} = 0$$

From symmetry we know that the potential should only be a function of r, which immediately simplifies our expression to:

$$\nabla^2\Phi = \frac{\partial}{\partial r}\left(r^2\frac{\partial\Phi}{\partial r}\right) = 0$$

This can be integrated to obtain Φ:

$$r^2\frac{\partial\Phi}{\partial r} = \int 0dr = k$$

$$\Phi = \int \frac{k}{r^2}dr \; = \frac{-k}{r} + C$$

Integrating twice has introduced two constants. To obtain the first constant C, we note that the zero point for this potential function is arbitrary. We may therefore freely set $\Phi(\infty) = 0$ and hence obtain $C = 0$. To obtain the second constant k we use a current conservation argument. The probe is injecting a current I, so by conservation the total current passing through a hemisphere centered at the probe should also be I. Now consider a differential volume element at a radius r from the tip (Figure A.1), with volume:

$$dV = dr \times rd\theta \times rsin\phi d\phi$$

This element has a resistance:

$$dR = \rho\frac{dr}{dA} = \frac{\rho dr}{r^2 sin\theta d\theta d\phi}$$

For a sufficiently small element, the potential across it is given by:

$$d\Phi = \frac{\partial\Phi}{\partial r} \times dr$$

Combining these results, we obtain the outward current through the element:

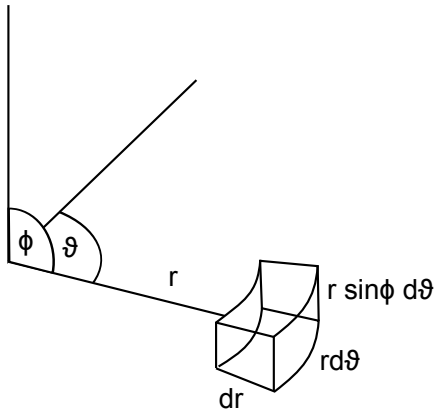


Figure A.1: **Differential volume element in spherical polar coordinates**

$$\begin{aligned} dI &= \frac{dV}{dR} \\ &= \frac{\partial}{\partial r}\Phi(r)dr / \frac{\rho dr}{r^2 sin\theta d\theta d\phi} \\ &= \frac{1}{\rho}\frac{\partial}{\partial r}\Phi(r)r^2 sin\phi d\phi d\theta \end{aligned}$$

Integrating over the hemisphere,

$$I = \int_0^{-\frac{\pi}{2}} \int_0^{2\pi} \frac{1}{\rho}\frac{\partial}{\partial r}\Phi(r)r^2 sin\phi d\phi d\theta$$

Recalling that $\frac{\partial\Phi}{\partial r} = \frac{k}{r^2}$, we have:

$$I = \frac{k}{\rho}\int 2\pi sin\phi d\phi = \frac{2\pi k}{\rho}cos\phi = -\frac{2\pi k}{\rho}$$

$$\Rightarrow k = -\frac{\rho I}{2\pi}$$

$$\boxed{\Phi(r)_{3D} = \frac{\rho I}{2\pi r}}$$

A.3 Φ on a 2-dimensional substrate

Current flow (and hence potential distribution) is different in a 2D substrate, with the current now spreading out in rings. Treating the Laplace equation in polar coordinates, and again assuming radial symmetry:

$$\nabla^2\Phi = \frac{\partial}{\partial r}\left(r\frac{\partial\Phi}{\partial r}\right) = 0$$

$$r\frac{\partial\Phi}{\partial r} = k$$

$$\Phi = \int \frac{k}{r} = kln(r) + C$$

Since the zero potential point is arbitrary and C is simply an offset, again let us set C=0. As for the 3D case, we obtain k from current conservation. With reference to Figure A.2:

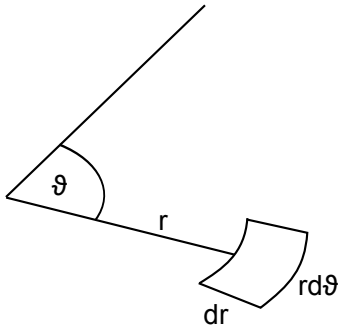


Figure A.2: **Differential element in polar coordinates**

$$dV = \frac{\partial\Phi(r)}{\partial r}dr$$

$$dR = \rho_s\frac{dr}{rd\theta}$$

$$I = \oint \frac{\frac{\partial\Phi(r)}{\partial r}dr}{\rho_s\frac{dr}{rd\theta}} = \int_0^{2\pi}\frac{kr}{\rho_s}d\theta = \frac{2\pi k}{\rho_s}$$

$$\Rightarrow k = \frac{\rho_s I}{2\pi}$$

$$\boxed{\Phi_{2D} = \frac{I\rho_s}{2\pi}ln(r)}$$

Note that this function becomes larger as r$\rightarrow\infty$ instead of going to zero like Φ_{3D}. As we will only be interested in potential *differences*, this will be of no concern.

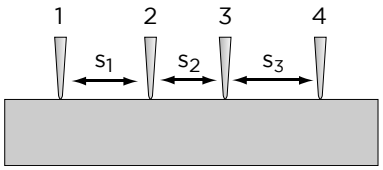


Figure A.3: **Collinear four probe measurement with unequal spacings**

A.4 Resistance → Resistivity

Now that we are in possession of expressions for the potential profile arising from single-probe current injection, let us use this to reach the main result: a mapping from four-terminal resistance to material resistivity. Begin by assuming that we have a 3D substrate. With reference to Figure A.3, suppose that we have four collinear probes (not necessarily equidistant) on this 3D substrate. If we inject a current from probe 1 which flows uniformly through the sample out to infinity, what potential difference is seen across the inner probes (2 & 3)?

$$\begin{aligned} V_{31} &= \text{potential at probe 3 due to current from probe 1} \\ &= \frac{\rho I}{2\pi r} \\ &= \frac{\rho I}{2\pi(s_1 + s_2)} \end{aligned}$$

Similarly,

$$V_{21} = \frac{\rho I}{2\pi(s_1)}$$

and so the potential difference across the two probes is:

$$\begin{aligned} \Delta V_1 &= V_{21} - V_{31} \\ &= \frac{\rho I}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_1 + s_2}\right) \end{aligned}$$

The same treatment if probe 4 is sourcing a *negative current* (or equivalently, draining a current which flows towards probe 4 from infinity) gives:

$$\Delta V_4 = \frac{\rho I}{2\pi}\left(\frac{1}{s_3} - \frac{1}{s_2 + s_3}\right)$$

In a four-probe resistance measurement we are doing both of these things - sourcing a current I through probe 1 and draining a current I through probe 4. By the superposition

theorem, the potential across the inner probes will simply be the sum of the two potentials derived above. And so we have:

$$\begin{aligned} R_{4PP,3D} &= \frac{V_{measured}}{I_{measured}} \\ &= \frac{\Delta V_1 + \Delta V_4}{I} \\ &= \frac{\rho}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2+s_1} + \frac{1}{s_3} - \frac{1}{s_2+s_3}\right) \end{aligned}$$

If the probe spacing is an equidistant s, this reduces to our familiar mapping:

$$\boxed{R_{4PP,3D} = \frac{\rho}{2\pi s}}$$

The process for obtaining the 2D correction factor is nearly identical, simply substituting the 2D surface potential expression:

$$\begin{aligned} R_{4PP,2D} &= \frac{V_{measured}}{I_{measured}} \\ &= \frac{\Delta V_1 + \Delta V_4}{I} \\ &= \frac{\rho_s}{2\pi}\Big(ln(s_1+s_2) - ln(s_1) + ln(s_2+s_3) - ln(s_3)\Big) \\ &= \frac{\rho_s}{2\pi}\left(ln\left[\frac{(s_1+s_2)(s_2+s_3)}{(s_1 s_3)}\right]\right) \end{aligned}$$

which under equidistant probe spacing reduces to:

$$\boxed{R_{4PP,2D} = \frac{\rho_s}{\pi} ln(2)}$$

A.5 Two-terminal resistances

Finally, we extend the same general technique to obtain an expression for the two-terminal resistance (excluding interfacial contact resistances). We now incorporate a finite probe radius r to avoid dividing by zero, and assume that the region underneath the probes has no resistance. As before, the total potential is given by a superposition. With reference to Figure A.4, in 3D we have

$$\Delta V_{measured} = V_{SD} + V_{DS} = 2\frac{\rho I}{2\pi}\left(\frac{1}{r} - \frac{1}{s-r}\right)$$

which accounts for the finite probe size - this is the potential between adjacent *edges* of the probes. To convert to a resistance we proceed as before:

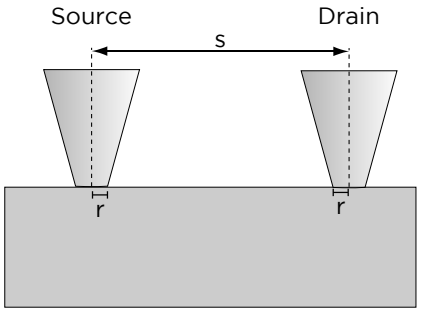


Figure A.4: **Two-terminal configuration with finite sized probes**

$$\boxed{R_{2T,3D} = \frac{V_{measured}}{I_{measured}} = \frac{\rho}{\pi}\left(\frac{1}{r} - \frac{1}{s-r}\right)}$$

The same analysis in 2D yields:

$$\Delta V_{measured} = V_{SD} + V_{DS} = 2\frac{\rho_s I}{2\pi}\Big(ln(s-r) - ln(r)\Big)$$

$$\boxed{R_{measured} = \frac{\Delta V_{measured}}{I} = \frac{\rho_s}{\pi} ln\left(\frac{s-r}{r}\right)}$$

Often in reality the condition $r \ll s$, is satisfied, which reduces these expressions to:

$$R_{2T,3D} = \frac{2\rho}{\pi r}$$

$$R_{2T,2D} = \frac{\rho_s}{\pi} ln\left(\frac{s}{r}\right)$$

These expressions give larger resistances than are usually quoted for spreading resistance (for example in Schroder[86]); the difference is that here we are interested in the resistance between two probes, not between a single probe and a contact at infinity.

Appendix B: Code Listings

B.1 Computing the propagated error from probe positioning errors

Referenced in Chapter 3, Section 3.1.2.3

Listing B.1: Language: Igor Pro scripting language

```
#pragma rtGlobals=1   // Use modern global access method.

//*******************************************************
function EvaluateError(s1,s2,s3,x,y,z)
//*******************************************************

// A propagator of error in co-linear 4PP measurements
// Four probes in a line have probe-to-probe separation of s1, s2, s3
// The error in this separation is x,y,z
// We can propagate the error in spacing into the error in resistivity by
    the method of partial derivatives.

variable s1,s2,s3   //Intended inter-probe spacings
variable x,y,z  //Errors in inter-probe spacings

// ERROR IN RESISTIViTY

variable Zero_Error_Expression =  (2*Pi) /  ((1/s1)+(1/s3) - (1/(s1+s2)) -
    (1/(s2+s3)) )

variable partial_s1 = ( 2*Pi*(s3^2)*((2*s1) + s2)*((s2+s3)^2) ) / (s2*(s1^2
     + s1*s2 + s3*(s2+s3))^2 )
variable partial_s2 = - (2*Pi* ( (1/((s1+s2)^2)) + (1/((s2+s3)^2)) ) ) /
    ((-(1/(s1+s3))+(1/(s1))-(1/(s2+s3))+(1/(s3)))^2 )
variable partial_s3 = (2*Pi*(s1^2)*((s1+s2)^2)*(s2+s3+s3)) / (s2*((s1^2)+(
    s1*s3) + s3*(s2+s3))^2)

variable Error = sqrt( (partial_s1^2) * (x^2)  + (partial_s2^2) * (y^2) + (
    partial_s3^2) * (z^2) )
```

```
print "In 3D, Rho = Resistance * ("+num2str(Zero_Error_Expression) + " +/-
    "+num2str(Error) + ")"
print "Relative error = "+num2str(Error*100/Zero_Error_Expression)+"%"

// Partial derivatives are obtained from WolframAlpha: {d/dx,d/dy,d/dz}  2*
    Pi / (ln((x+y)/(x)) + ln((y+z)/(z)))

Zero_Error_Expression=2*Pi / (ln((s1+s2)/(s1)) + ln((s2+s3)/(s3)) )

partial_s1 = ( 2*Pi*s2) / (s1*(s1+s2)*( ln((s1+s2)/s1) + ln((s2+s3)/s3) )
    ^2)
partial_s2 = ( 2*Pi*( (1/(s1+s2) + 1/(s2+s3) )  ) ) / ((ln((s1+s2)/s1)+ln((
    s2+s3)/s3)   )^2)
partial_s3 =  ( 2*Pi*s2) / (s3*(s2+s3)*( ln((s1+s2)/s1) + ln((s2+s3)/s3) )
    ^2)

Error = sqrt( (partial_s1^2) * (x^2)  + (partial_s2^2) * (y^2) + (
    partial_s3^2) * (z^2) );
print "In 2D, Rho = Resistance * ("+num2str(Zero_Error_Expression) + " +/-
    "+num2str(Error) + ")"
print "Relative error = "+num2str(Error*100/Zero_Error_Expression)+"%"


// ERROR IN RESISTANCE


Zero_Error_Expression=(1/(2*Pi)) * ((1/s1)+(1/s3) - (1/(s1+s2)) - (1/(s2+s3
    )) )

partial_s1 = ( 1/((s1+s2)^2) - 1/(s1^2) ) / (2*Pi)
partial_s2 =( 1/((s1+s2)^2) - 1/((s2+s3)^2) ) / (2*Pi)
partial_s3 = ( 1/((s2+s3)^2) - 1/(s3^2) ) / (2*Pi)

Error = sqrt( (partial_s1^2) * (x^2)  + (partial_s2^2) * (y^2) + (
    partial_s3^2) * (z^2) );
print "In 3D, R = Rho * ("+num2str(Zero_Error_Expression) + " +/- "+num2str
    (Error) + ")"
print "Relative error = "+num2str(Error*100/Zero_Error_Expression)+"%"


Zero_Error_Expression=(1/(2*Pi)) * (ln((s1+s2)/(s1)) + ln((s2+s3)/(s3)) )

partial_s1 = - s2 / ( 2*Pi*s1^2 + 2*Pi*s1*s2 )
partial_s2 = (1/(s1+s2) + 1/(s2+s3 ))   / (2*Pi)
partial_s3 =  - s2 / ( 2*Pi*s2^s3 + 2*Pi*s3^2 )

Error = sqrt( (partial_s1^2) * (x^2)  + (partial_s2^2) * (y^2) + (
    partial_s3^2) * (z^2) );
```

```
print "In 2D, R = Rho * ("+num2str(Zero_Error_Expression) + " +/- "+num2str
    (Error) + ")"
print "Relative error = "+num2str(Error*100/Zero_Error_Expression)+"%"

end
```

B.2 Simulating carrier density freezeout

Referenced in Chapter 3, Section 3.2.4

Listing B.2: Language: Igor Pro scripting language

```
#pragma rtGlobals=1   // Use modern global access method.

//*******************************************************
Function Generate_Ntype_Freezeout_Curve(DopingDensity_cm3,
    IonizationEnergy_eV,EffectiveMass,Bandgap_eV)
//*******************************************************

  //-----------------------------------------------------
  // Declare & initialize waves and variables to be used
  //-----------------------------------------------------
  variable DopingDensity_cm3, IonizationEnergy_eV,EffectiveMass,Bandgap_eV
  variable Temperature,jj,kk;

  variable ElectronMass = 9.10938e-31
  variable Boltzmann_J = 1.381e-23
  variable Boltzmann_eV = 8.617e-5
  variable Planck = 6.626e-34
  variable m3_to_cm3 = 1e-6

  // Taken out of the loop for efficiency
  variable Precalculation = 2*Pi*EffectiveMass*ElectronMass*Boltzmann_J /(
      Planck)^2

  // These waves are used to calculate the Fermi energy at each
  // temperature step. Use a lot of points for good precision
  Make/N=1500000 FermiEnergy_eV = x/1e6
  Make/N=1500000 Difference = 0
  Make/N=1500000 IonizedDensity_cm3 = 0
  Make/N=1500000 ElectronDensity_cm3 = 0

  // These waves store the Fermi energy and carrier density at each
  // temperature step
  Make/N=4000 TempDependent_Ef = NaN
  Make/N=4000 TempDependent_Density_cm3 = NaN

  //-------------------------------------------------------------
  // Begin solving loop:
  // For a temperature range 20 .. 400K in steps of 1K,
  //  Calculate the density of ionized dopants
  //  Calculate the density of free electrons
  //  Identify the Fermi energy value for which charge neutrality
  //  is satisfied
  //    (Note that we don't bother calculating the minority
  //    carrier density. This will always be many orders of
```

```
    //    magnitude less than the ionized donor density)
    //  Store this energy together with the carrier density
    //-------------------------------------------------------------

    for(Temperature=4000;Temperature>300;Temperature=Temperature-10)
      IonizedDensity_cm3=DopingDensity_cm3 / (1+(2*exp((FermiEnergy_eV-(
          Bandgap_eV-IonizationEnergy_eV))/((Boltzmann_eV*(Temperature/10)))))
          )
      ElectronDensity_cm3= (2*(Precalculation*(Temperature/10))^(3/2))*exp((
          FermiEnergy_eV-Bandgap_eV)/((Boltzmann_eV*(Temperature/10))))*
          m3_to_cm3

      // The point of intersection is taken as the minima of the difference
          between the two waves.
      Difference=abs(IonizedDensity_cm3 - ElectronDensity_cm3)
      wavestats/Q Difference
      TempDependent_Ef[Temperature]=V_minloc/1e6
      TempDependent_Density_cm3[Temperature]=ElectronDensity_cm3[V_minloc]
      print Temperature
    endfor
end

//*******************************************************
Function Generate_Ptype_Freezeout_Curve(DopingDensity_cm3,
    IonizationEnergy_eV,EffectiveMass,Bandgap_eV)
//*******************************************************

    //-----------------------------------------------------
    // Declare & initialize waves and variables to be used
    //-----------------------------------------------------
    variable DopingDensity_cm3, IonizationEnergy_eV,EffectiveMass,Bandgap_eV
    variable Temperature,jj,kk;

    variable ElectronMass = 9.10938e-31
    variable Boltzmann_J = 1.381e-23
    variable Boltzmann_eV = 8.617e-5
    variable Planck = 6.626e-34
    variable m3_to_cm3 = 1e-6

    // Taken out of the loop for efficiency
    variable Precalculation = 2*Pi*EffectiveMass*ElectronMass*Boltzmann_J /(
        Planck)^2

    // These waves are used to calculate the Fermi energy at each
    // temperature step. Use a lot of points for good precision
    Make/N=1500000 FermiEnergy_eV = x/1e6
    Make/N=1500000 Difference = 0
    Make/N=1500000 IonizedDensity_cm3 = 0
    Make/N=1500000 HoleDensity_cm3 = 0
```

```
  // These waves store the Fermi energy and carrier density at each
  // temperature step
  Make/N=4000 TempDependent_Ef = NaN
  Make/N=4000 TempDependent_Density_cm3 = NaN

  //-----------------------------------------------------------------
  // Begin solving loop:
  // For a temperature range 20 .. 400K in steps of 1K,
  //  Calculate the density of ionized dopants
  //  Calculate the density of free electrons
  //  Identify the Fermi energy value for which charge neutrality
  //  is satisfied
  //    (Note that we don't bother calculating the minority
  //    carrier density. This will always be many orders of
  //    magnitude less than the ionized donor density)
  //  Store this energy together with the carrier density
  //-----------------------------------------------------------------

  for(Temperature=4000;Temperature>300;Temperature=Temperature-10)
    IonizedDensity_cm3=DopingDensity_cm3 / (1+(4*exp((FermiEnergy_eV-(
        Bandgap_eV-IonizationEnergy_eV))/((Boltzmann_eV*(Temperature/10)))))
        )
    ElectronDensity_cm3= (2*(Precalculation*(Temperature/10))^(3/2))*exp
        ((0-FermiEnergy_eV)/((Boltzmann_eV*(Temperature/10))))*m3_to_cm3

    // The point of intersection is taken as the minima of the difference
        between the two waves.
    Difference=abs(IonizedDensity_cm3 - ElectronDensity_cm3)
    wavestats/Q Difference
    TempDependent_Ef[Temperature]=V_minloc/1e6
    TempDependent_Density_cm3[Temperature]=ElectronDensity_cm3[V_minloc]
    print Temperature
  endfor
end
```

B.3 Simulating the diffusion of a δ-doping profile

Referenced in Chapter 4, Section 4.2.0.3

Listing B.3: Language: Igor Pro scripting language

```
#pragma rtGlobals=1   // Use modern global access method.

//*******************************************************
Function IntrinsicDiffuse(Temperature,DiffusionTime)
//*******************************************************

//-------------------------------------------------------------
// Declare & initialize waves and variables to be used
//-------------------------------------------------------------
variable Temperature  //In Celsius
variable DiffusionTime  // In seconds
Temperature=Temperature+273.15  //Convert to Kelvin for internal use

 //External waves to store the output
WAVE Distance   // In nm.  Must be manually set to an appropriate range;
    start with a 2e6 point wave scaled to +/- 1e-7
WAVE Concentration

variable k=8.617e-5

// Diffusion constants from Gossman - Delta doping in silicon (Crit. Rev.
    Solid State. Mater. Sci 1993)
variable D1_0 = 3.85
variable E1_A = 3.66
variable D2_0 = 4.44
variable E2_A = 4.00
variable D3_0 = 44.2
variable E3_A = 4.37

variable D=D1_0* exp(- E1_A/(k*Temperature))  + D2_0* exp( -E2_A/(k*
    Temperature)) + D3_0* exp( -E3_A/(k*Temperature))
print "Intrinsic diffusivity = "+num2str(D)+" cm2s-1"

// Fickian diffusion (fixed source, both directions)
Concentration = (1 / (2 * sqrt(Pi * D * DiffusionTime) ) ) * exp( - (
    Distance*1e-7*Distance*1e-7)/(4*D*DiffusionTime))

// Normalise it:
wavestats/Q Concentration
Concentration=Concentration/V_Sum

// Compute FWHM
CurveFit/NTHR=0 gauss  Concentration /X=Distance /D
Wave W_coef
```

```
print "Profile broadened to FWHM of "+num2str(2*sqrt(ln(2))*W_coef[3])+" nm
    "

end

//*******************************************************
Function ExtrinsicDiffuse(Temperature,DiffusionTime)
//*******************************************************

//-------------------------------------------------------
// Declare & initialize waves and variables to be used
//-------------------------------------------------------
variable Temperature  //In Celsius
variable DiffusionTime  // In seconds
Temperature=Temperature+273.15  //Convert to Kelvin for internal use

//External waves to store the output
WAVE Distance       // In nm.  Must be manually set to an appropriate range
    ; start with a 2e6 point wave scaled to 1e-2
WAVE Concentration

variable k=8.617e-5

// Diffusion constants from Gossman - Delta doping in silicon (Crit. Rev.
    Solid State. Mater. Sci 1993)
variable D1_0 = 3.85
variable E1_A = 3.66
variable D2_0 = 4.44
variable E2_A = 4.00
variable D3_0 = 44.2
variable E3_A = 4.37

variable n_d =3e21 //Total number of dopants (relevant for extrinsic
    diffusion)
variable n_i = 1.01e17*((Temperature)^(3/2))*exp(-0.68/(k*Temperature)) //
    approximation of intrinsic density
print "Instrinsic carrier density at "+num2str(Temperature-273.15)+"
    celsius is approximately "+num2str(n_i)+" cm-3"

variable D = 2*( D1_0 * exp(-E1_A / (k*Temperature)) + D2_0 * exp(-E2_A / (
    k*Temperature))*(n_d/n_i)  + D3_0 * exp(-E3_A / (k*Temperature)) *(n_d/
    n_i)*(n_d/n_i))
print "Extrinsic diffusivity = "+num2str(D)+" cm2s-1"

// Fickian diffusion (fixed source, both directions)
Concentration = (1 / (2 * sqrt(Pi * D * DiffusionTime) ) ) * exp( - (
    Distance*1e-7*Distance*1e-7)/(4*D*DiffusionTime))

// Normalise it:
```

```
    wavestats/Q Concentration
    Concentration=Concentration/V_Sum

    // Compute FWHM
    CurveFit/NTHR=0 gauss  Concentration /X=Distance /D
    Wave W_coef
    print "Profile broadened to FWHM of "+num2str(2*sqrt(ln(2))*W_coef[3])+" nm
        "

    end
```

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